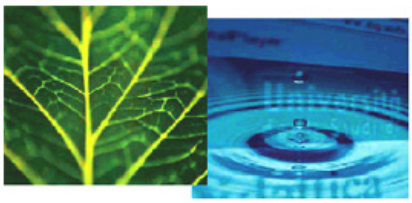

International Doctorate School in Information and Communication Technologies

DIT - University of Trento

SMART CMOS IMAGE SENSOR FOR 3D MEASUREMENT

Vanam Upendranath

Advisor:

Alessandro Zorat,

Professor, ICT,

Università degli Studi di Trento, Trento.

Co-Advisor:

Ing. Massimo Gottardi,

Senior Researcher, MIS, SOI,

ITC-irst, Trento.

February 2005

DIT-05-021

Abstract

3D measurements are concerned with extracting visual information from the geometry of visible surfaces and interpreting the 3D coordinate data thus obtained, to detect or track the position or reconstruct the profile of an object, often in real time. These systems necessitate image sensors with high accuracy of position estimation and high frame rate of data processing for handling large volumes of data. A standard imager cannot address the requirements of fast image acquisition and processing, which are the two figures of merit for 3D measurements. Hence, dedicated VLSI imager architectures are indispensable for designing these high performance sensors. CMOS imaging technology provides potential to integrate image processing algorithms on the focal plane of the device, resulting in smart image sensors, capable of achieving better processing features in handling massive image data.

The objective of this thesis is to present a new architecture of smart CMOS image sensor for real time 3D measurement using the sheet-beam projection methods based on active triangulation. Proposing the vision sensor as an ensemble of linear sensor arrays, all working in parallel and processing the entire image in slices, the complexity of the image-processing task shifts from O (N^2) to O (N). Inherent also in the design is the high level of parallelism to achieve massive parallel processing at high frame rate, required in 3D computation problems. This work demonstrates a prototype of the smart linear sensor incorporating full testability features to test and debug both at device and system levels.

The salient features of this work are the asynchronous position to pulse stream conversion, multiple images binarization, high parallelism and modular architecture resulting in frame rate and sub-pixel resolution suitable for real time 3D measurements.

Keywords*: Smart CMOS image sensor, 3D measurement, sub-pixel resolution, multiple threshold image binarization***,** *active triangulation*

Contents

Acknowledgements

"Endaro mahaanu bhaavulu, andariki vandanamulu", in my mother tongue, Telugu, says there are 'so many great people, I salute them all'.

First of all, I am deeply indebted to Prof. Zorat, my advisor, for his kind guidance, constant encouragement and unwavering support during my entire Ph. D program. He has given me several opportunities for professional growth and has always come to my rescue during crisis periods.

I am running short of words to express deep appreciation to my co-advisor, Ing. Massimo Gottardi, for sparing me countless hours of his precious time during all the stages of my research. But for his guidance and untiring efforts, I would not have completed my work. I will always be grateful to him.

I thank the Dean ICT and the Head, DIT for providing me an opportunity to be on the rolls of ICT.

I thank Prof. Giancarlo Parodi, University of Genova and Prof. Alessandro Paccagnelia to be on my committee and accepting to review my thesis.

I thank Dr. Mario Zen, Director, ITC-irst for permitting me to work with the disciplined and professional environment of the Microsystems group. I thank Dr. Simoni, group leader, SOI, for providing me the Cadence facilities and sponsoring the fabrication of the prototype of my chip. I thank Drs. Lorenzo and David, Nicola, the Viarani brothers, Fabrizio, Stefano, Malfatti and all the members of Microsystems group for helping me whenever I have approached them. This is the friendliest environment I have ever seen. I thank Dr. Dalla Betta and Professor Soncini for introducing me to the group.

I thank Prof. Andreas Andreou and his illustrious group at Johns Hopkins University, Baltimore, USA, for providing me a wonderful opportunity to work with them in the eminent "Andreou lab". I am always grateful to Prof. Andreas for his kind and exceptional support. My special thanks are due to Philips, Eugenio, Frank and Professors: Ralph-Etienne-Cummings, Paul Sotiriadis and their teams for their support while in JHU.

I also had to face the saddest moment in my life during this program- the sudden demise of my father. The stay in JHU has helped me overcome great part of the grief. The Badminton team at JHU has helped me come out of the solitude.

I thank Mr. Oleg for his timely help in FPGA and VHDL design part of my thesis. I thank all the faculty members, supporting staff and friends in DIT, CISCA, Secretariat, Ph. D office and Welcome office for their prompt support. Thanks are also due to all the colleagues at ICT, University of Trento, ITC-irst and CEERI Pilani for their support.

I would like to thank the peers in the field, through this medium, who have been magnanimous to respond to my queries: Prof. Varanasi and Dr. Harvey Glass, USF; Prof. Sangiovanne Vincentelli, UCB; Prof. Ran Ginosar, Technion; Prof. Paul Allen, GIT; Prof. A.J.P. Theuwissen, Prof. Harry Veendrick and Dr. Ad Peeters, Philips Research; Dr. Alireza Moini, Univ. of Adelaide; Prof. Brian Curless, UW ; Dr. B. Pain, JPL; Ken Chapman & Peter Alfke, Xilinx, Dr. Angelo Beraldin, NRC, IIT, Canada, Y.Oike, Tokyo Univ… and the list is endless. I seek forgiveness from those who spared their professional time to answer me patiently, but whose names I could not mention here.

I thank Director, CEERI, Pilani, and DG-CSIR, India, for their extraordinary gesture in granting me study leave to pursue my Ph. D program in Italy.

I finally thank all my family members in India and USA for their moral support. Special words of appreciation to my wife Padma, and sons Vijayendra and Sai Srinath for allowing me to pursue this venture at a rather late(r) part of life, in a far off land and sustaining on their own during such a long separation. I always remember Italy as the most beautiful country with friendliest people. Trento has been my dream city and truly a home away from home.

Trento , 10th January 2005 Vanam Upendranath

Chapter 1

Introduction

Vision is our most powerful sense, which provides us with a remarkable amount of information about our world in three dimensions. It facilitates us to interact with our surroundings intelligently, learn the position and identities of objects and the relationship between them, without requiring any physical contact. Hence, efforts to provide machines a sense of vision to see and react to the situation has always been the thrust in the vision research [BER1].

3D measurements form a major part of vision research. They enable extraction of the 3D coordinate data by means of an image-sensing medium, from the geometry of visible surfaces of the target, and reconstruct its profile information. Examples of 3D measurement applications abound- a robot picking an object, a space probe collecting samples, an inspection system detecting the solder paste deposits in an electronic assembly, or a shape reconstruction task of a museum object, all require accurate object position or range estimation, often in real time. To capture the complete shape of an object, thousands of samples must be acquired, for which a suitable method of measurement and a high speed and accurate image sensor are necessary for reliable image acquisition and processing. While the image from a camera shows the intensity distribution of the viewed scene, a range camera, in contrast, gives the distance from the camera to the objects of the scene.

The range-imaging sensors in such systems are unique imaging devices in that the image data points explicitly represent scene surface geometry as sampled surface points. The inherent problems of automatically interpreting 3-D structure from the output of other types of imaging devices, such as video cameras, are not encountered with range-imaging sensors. Range images are also known as range map, depth map, depth image, range picture, 3-D image etc., depending on the context [BES].

1.1 Optoelectronic methods of 3D imaging

Several optoelectronic techniques for 3D imaging have been proposed in the literature for range imaging: the surveys of [BES, JAR] for range detection are the classic references for 3D imaging researchers. [STR] covered range-imaging techniques from an optical engineering viewpoint. More recently different other taxonomies are proposed: while [CUR] suggests different active methods, [DAV] proposes a new classification to unify a class of methods in terms of spatial vs. temporal methods.

Range images are obtained in many different ways. Traditionally these are classified into two categories, active and passive range imaging. Figure 1.1 shows one such classification. While the passive rely on ambient environment conditions, the active method uses a coherent light source to project onto the object in a structured manner and determines the shape of the object by its reflections. Passive systems require well-defined features such as targets and edges and have difficulty with sculptured surfaces and unstructured environments. The computer vision research community is largely focused on passive methods, which extract shape from digitized images, including shape-from-shading for single images, stereo methods for pairs of images, and optical flow methods for video streams [CUR]. Whereas these methods require very little special purpose hardware, they typically do not yield dense and highly accurate digitizations required by a number of applications.

1.1.1 Active optical methods

Since the active optical systems provide their own illumination, they can easily measure surfaces in most environments. In contrast to passive methods, many active optical rangefinders can rapidly acquire dense, highly accurate range samplings. The active optical systems sample the shape of an object along a set of regularly spaced lines of light, yielding a grid of depths known as a range

image. These active optical methods include time of flight (ToF), interferometry and triangulation. The following discussion brings out salient features of each method.

1.1.1 .1 Time of flight method

In ToF [LAN, ULL, VIA] systems, a projected light is reflected from a target object with some delay proportional to the distance. A camera detects the arrival time of the reflected light to measure the distance. However, despite its apparent simplicity, a laser ToF system is not easy to design in practice. Primarily, the coincidence electronics must accurately measure very short time intervals. Secondly, the power received from the target surface may be very low, which means that the electronic signal generated by the photodetector may be affected by noise [POU]. Thus, the surface property and orientation along with range affect the energy collected by the photodetector. This limits the range accuracy typically to a few centimetres. For smaller objects of <1m in size, attaining 1 part per 1000 accuracy with time-of-flight methods require very high speed timing circuitry, because the time differences to be detected are in the femto second (10^{-15} s) range. Hence, this method is generally applied in long-range 3-D measurement of large objects, such as monuments and buildings.

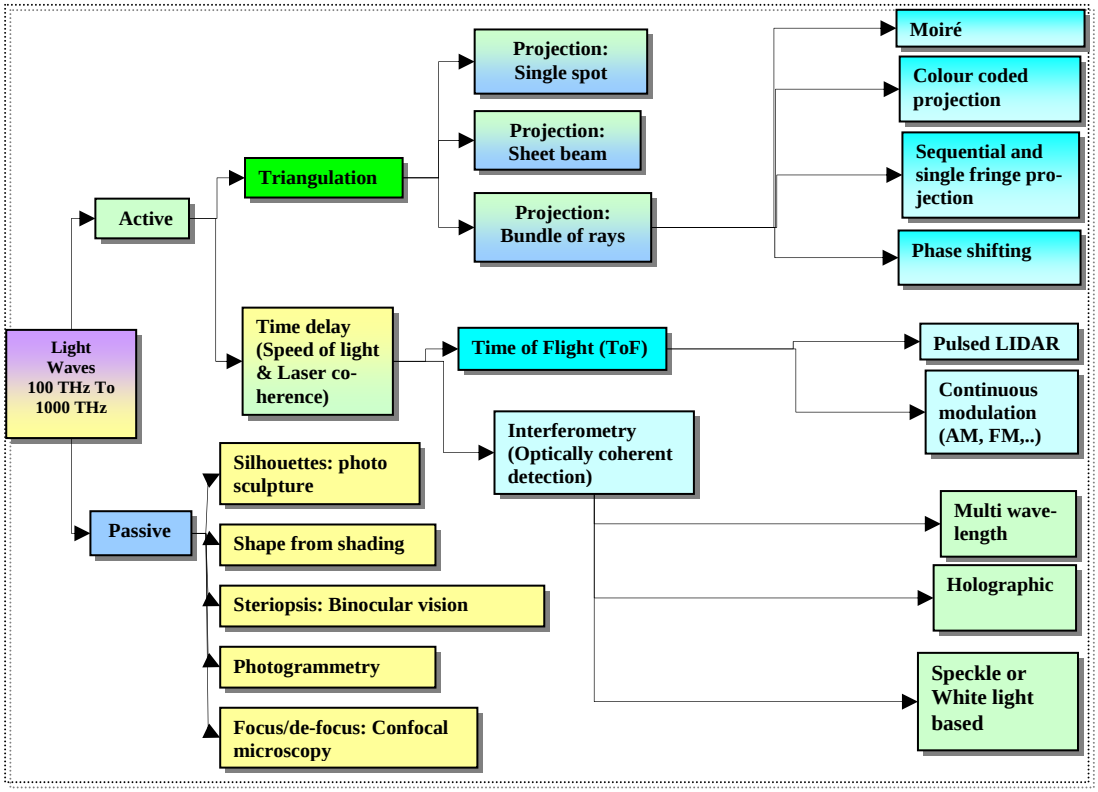

Figure 1.1: *Optoelectronic techniques for 3D imaging*

1.1.1.2 Interferometric method

In the interferometric method [BES], a spatially or temporally varying periodic pattern is projected on to the surface of the object. The reflected light is mixed with a reference pattern, which demodulates the signal to reveal the variations in surface geometry. While, moire interferometry involves the projection of coarse, spatially varying light patterns onto the object, the holographic interferometry relies on mixing coherent illumination with different wave vectors to achieve the objective. The angular separation of source and detector is critical to range measurements and therefore, moire can be considered another type of triangulation method though it exhibits many similarities to holographic interferometry. Moire methods can have phase discrimination problems when the surface does not exhibit smooth shape variations, which limits the maximum slope the surface can have to avoid ranging errors.

1.1.1.3 Optical triangulation method

Optical triangulation is one of the most well known optical rangefinding approaches. In this method, the location of the centre of the reflected light pulse imaged on the sensor corresponds to a line of sight that intersects the illuminant in exactly one point, yielding a depth value. By translating or rotating the object through the beam or by scanning the beam across the object, the shape of the object can be acquired.

[RIO] presents an innovative approach to triangulation-based range imaging, which shows a synchronized scanning scheme. It allows very large fields of view with small triangulation angles and with high precision. With smaller triangulation angles, a reduction of shadow effects is inherently achieved. The idea is to synchronize the projection of the laser spot with its detection. The instantaneous field of view of the position detector follows the spot as it scans the scene. The focal length of the lens is therefore related only to the desired depth of field or measurement range and not to the field of view. With optical synchronization, an improvement in ambient light immunity due to a small instantaneous field of view (long focal lengths) and a reduction of speckle noise (through spatial filtering) are achieved [BER3]. The basic optical configuration for this large field of view 3D digitizer, is shown in Figure 1.2.

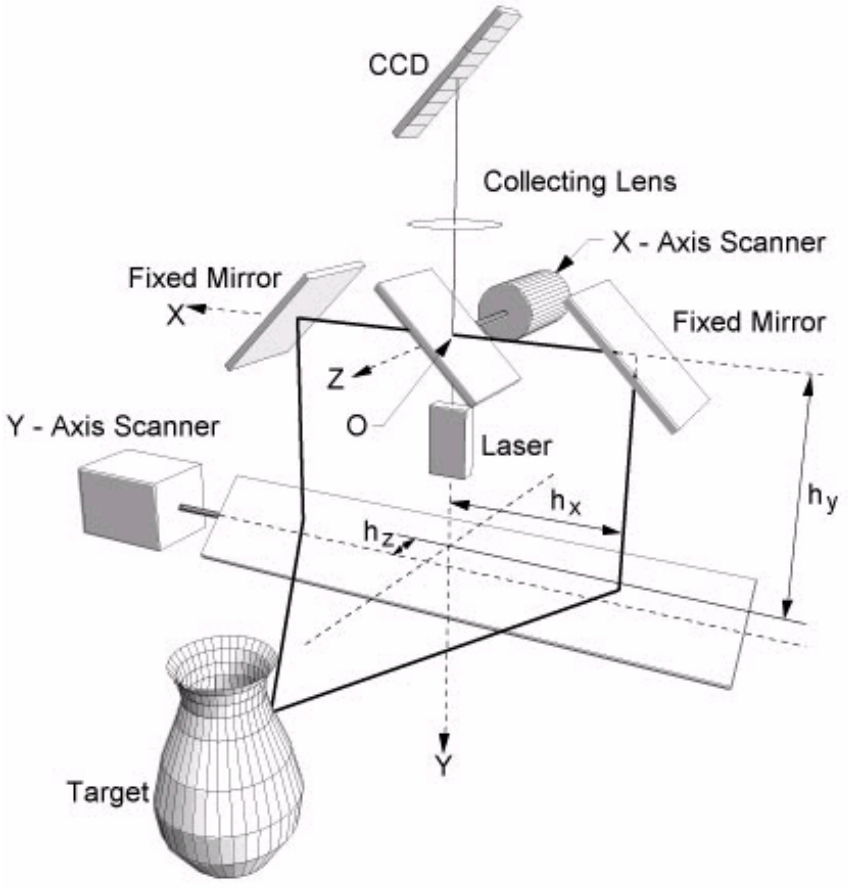

Figure 1.2: *Auto-synchronized scanner: dual-scan axis (used equally in triangulation and time of flight systems) CNR [BER3]*

Both mirrors are driven by galvanometers. A raster imaging mode produces a range image of the scene: the x-axis scanner (fast axis) is used for the line scanning while the y-axis (slower speed) deflects vertically the scanned beam to produce a raster image. A 3D surface map is obtained by scanning a laser beam onto a scene, collecting the light that is scattered by the scene in synchronism with the projection mirrors,

and finally, focusing this light onto a linear position detector. The image acquisition process yields three quantities per sampling interval: two angular positions of the mirrors and the position of the laser spot on the linear position detector. The equations obtained after the calibration process are used to map the angular position of the mirrors and the laser spot position into (*x, y, z*) coordinates.

1.2 Comparison of basic active optical measurement methods

The three basic active optical measurement principles: triangulation, interferometry ToF are compared in Figure 1.3, in terms of distance, range and resolution illustrating their suitability for specific applications. The most critical parameters of thes systems are the depth measuring range z and the depth resolutions δz. The figure illustrates the measuring and resolution ranges that are covered by the existing measuring systems. The highest absolute resolutions are achieved by interferometry, which reaches accuracies of λ/100 and can measure ranges up to 10 m using multi-wavelength techniques [CUR]. However, these are very expensive systems. Active triangulation can be used with high resolution from the millimetre range up to several meters where the accuracy depends mainly on depth of field and can be < 10µm for small depths. The ToF techniques allow measurement of depths in the range from tens of cm up to tens of km, but as noted above, the design of these systems could be very challenging [SIM].

All the rangefinding techniques presented here have their specific advantages and drawbacks and none can be considered an overall "optimal" choice [POU]. The 3-D vision system designer must chose the technique best suited for his / her needs. The accuracy and acquisition time are two important issues that a designer has to consider along with the physical dimensions of the rangefinder, which is often of importance, particularly in robotics applications.

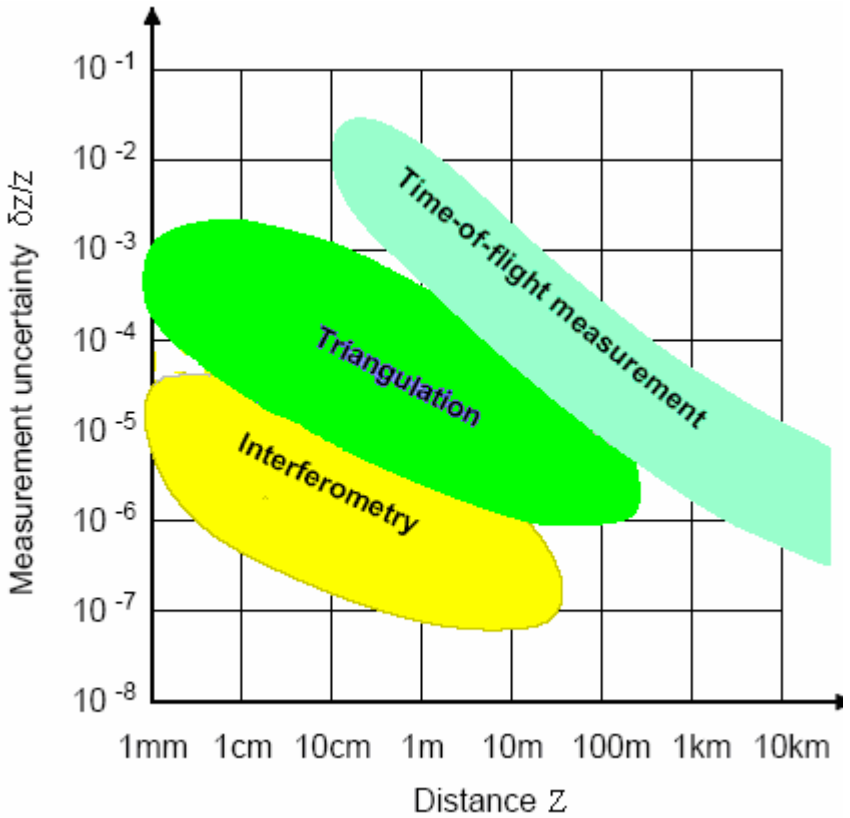

Figure 1.3: *Performance map showing relative resolution of active 3D optical measurement methods [SCH]*

Though in the past the triangulation systems were considered inaccurate or slow, the state of the systems have become accurate, fast, and compact, mainly owing to the advent of synchronous scanning approaches. Triangulation systems go from sequential, as in point scanners, to parallel, as in the

intensity ratio scheme or the color encoded sheet beam scheme. Triangulation systems have been the stronghold of range imaging, and promise to remain so [BES].

Since active triangulation using the sheet beam method is the basis of this thesis, it is discussed in detail in the following sections.

1.3 Active optical triangulation method

In the active triangulation method, the scene is illuminated by a coherent light source from one direction and viewed from another [BES, JAR, MUN, RIO]. Figure 1.4 shows a typical triangulation system and range imaging configuration in 2D. The illumination angle θ, the viewing angle α, and the baseline between the illuminator and the sensor are the triangulation parameters. The variety of the active triangulation methods differ primarily in the structure of the illuminant, viz., a single spot or a sheet beam (also known as stripe or sheet of light) or coded light, and the dimensionality of the sensor (linear sensor or 2D structure) and the scanning method, moving the object or moving the scanning mechanism. The shape of the object is acquired by translating or rotating the object through the beam or by scanning the beam across the object.

[DAV] suggests that unifying the various triangulation methods within the space-time [CUR] framework allows new hybrid algorithms, ex: temporal stereo, for improved reconstruction of static scenes with unstructured varying (intensity) lighting.

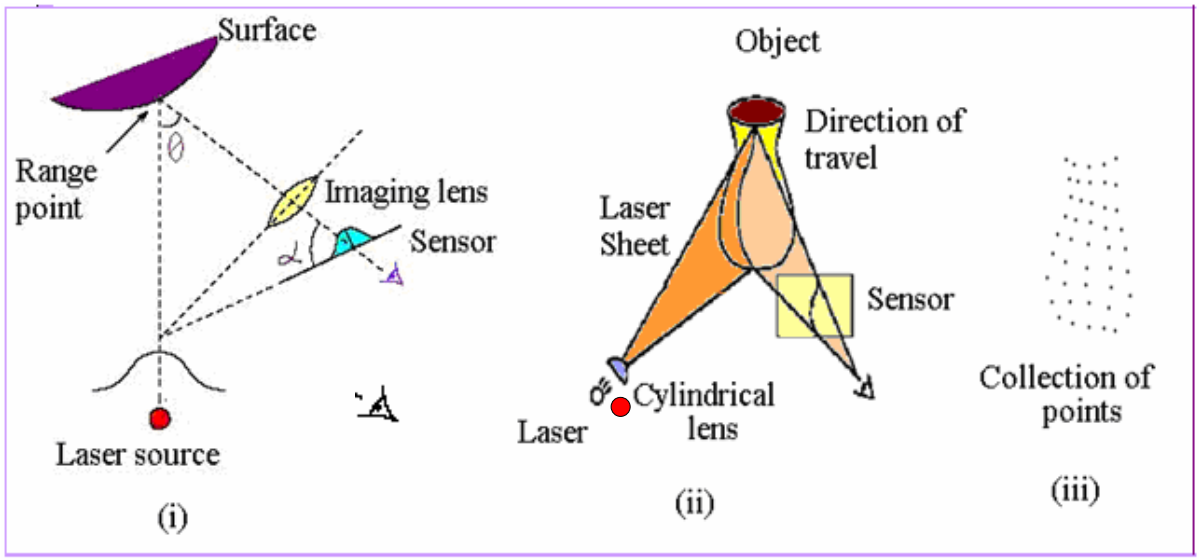

Figure 1.4: *Optical triangulation and range imaging showing (i) the triangulation setup in 2D giving a range value (ii) The 3D setup giving the range image and (iii) the collection of points showing the range map of the object [CUR]*

Figure 1.5 shows the structure of the data, which can be (i) a spot or (ii) a profile of the shape or (iii) a range map of the object. A beam of light forms a spot on the surface and provides a single range value. By passing the beam through a cylindrical lens, a light stripe can be projected onto an object to collect the

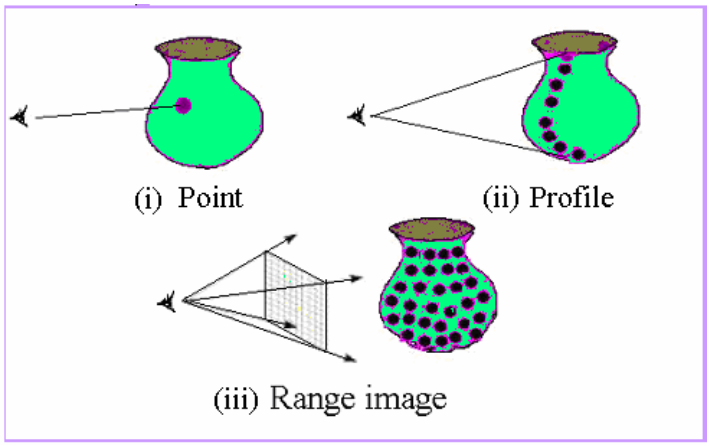

Figure 1.5: *Structure of data showing point, profile and range imaging concepts [CUR]*

range profile and by projecting multiple spots or sheets of light, a range map can be obtained. It may be noted here that frames per sec. (fps) denotes position detection rate on the sensor focal plane. For example, to achieve 100 x 100 range data for a range map, a range map needs 100 frames for position detection of a scanning sheet beam. 1k fps (frame access rate/position detection rate) corresponds to 10 range maps/s.

1.3 Image sensors in 3D measurement

While the 2D vision is concerned with interpreting a three dimensional environment under a specific illumination in other words an intensity profile of light, the 3D vision is concerned with extracting information from the geometry and the texture of the visible surfaces in a scene. Though the 2D methods are used with reasonable success [SIM] in several industrial applications (ex: whole and partial body scans, reverse engineering of industrial components, reproduction of rare objects, object presence and positioning etc.,) for acquiring and interpreting the 3D data, this mechanism gives only limited information about the detailed shape of an object.

Being the core of a 3D measurement system, an image sensor is required to handle the image acquisition and processing efficiently where speed and accuracy are both critical. A very high frame rate is necessary to reconstruct a range map, which requires thousands of frames per second (fps). For instance, using a spot beam X-Y scanner, a range map with 1M pixels (1024×1024 pixels) requires 1M position detections per range map in a 3D measurement system. Thus, 30M fps position detection is necessary for 30-range maps/s range finding with 1M pixels. A sheet beam scanner can reduce the number of frames for a range map; however, 30k fps position detection are needed to realize a real-time range finding system. Several high-speed CMOS image sensors are reported in the literature, ex: [KLE, KRY], with parallel ADCs realizing a maximum of 500- 2000 fps [OIK1].

Since the two important requirements of image acquisition and processing are difficult to meet with standard imagers, it is necessary to develop dedicated vision chips [BRA3, NEZ1, OIK1] with on-chip visual signal processing for achieving the real time functionality in 3D. To achieve this in 3D, generally a 2D imager with *specific processing capabilities* (known as smart features to address the needs of different applications) performing at very high frame rate is mandatory. CMOS technology enables the development of these sensors a possibility.

1.3.1 CMOS technology for image sensors

While *CMOS is the heart of the electronics industry, the image sensors are the eyes* of a whole range of products from toys to complex space stations. With the availability of sub-micron CMOS technologies for

imaging, in terms of the following benefits, a great interest has been focused in recent times on the development of specialised image sensors [MOI, FOS]:

• **Mature technology**: CMOS processes have been available for long period and are well developed and well established.

• **Design resources**: Many design libraries for circuit and logic are supported by various research groups and industries and are readily available for incorporating in the user applications.

• **Accessibility**: There are many fabs around the world, to fabricate prototype designs at lower prices.

• **Fabrication cost**: Because CMOS process is standardized, the fabrication of CMOS designs is less expensive, compared to other process technologies.

• **Power consumption**: As CMOS technology scales down, the downscaling of the power supply follows a similar trend, resulting in lower power consumption.

• **Compatibility with VLSI circuits**: Since CMOS technology is already optimized for logic and memory, it is relatively easy to integrate VLSI circuits with CMOS image sensors.

1.3.2 Smart image sensors or vision sensors

The integration of photosensitive devices with visual information processing elements on the same substrate of the device, known as smart image sensors or vision sensors (MOI), represents a select area in machine vision where high performance in terms of frame rates, accuracy and resolution are the most demanding features. (It may be noted the terminology ‘ smart image sensors’ and ‘vision sensors’ are interchangeably used in this thesis).

A smart sensor is well defined in *“Vision Chips”* by [MOI] as following:

“Smart sensors refer to those devices in which the sensors and circuits co-exist, and their relationship with each other and with higher-level processing layers goes beyond the meaning of transduction. Smart sensors are information sensors, not transducers and signal processing elements. Everything in a smart sensor is specifically designed for the application targeted for.”

In this thesis, the concept of smart image sensors is further focused on the aspect of the devices in which image sensors and visual processing circuits (beyond signal processing) co-exist, and they interact with each other in order to increase the functionality of the imager chip and the quality of processing.

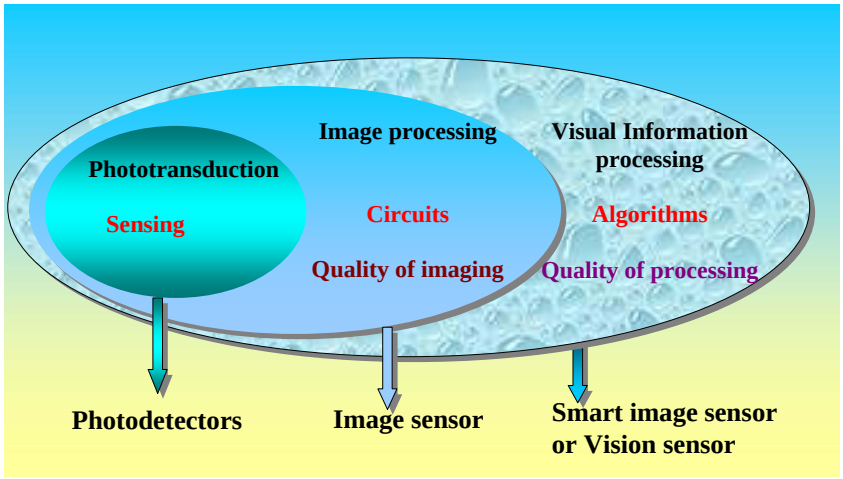

Figure 1.6: *Conceptual block diagram of a vision sensor*

Figure 1.6 shows the conceptual block diagram of a vision sensor. While detecting light intensity and transducing it to electrical parameter (phototransduction) is performed by photodetectors (photodiodes, photogates etc.), signal processing circuits such as correlated double sampling (CDS) [WHI], dynamic range enhancement, on-chip clock generation (widely used in camera applications) etc., [DIC1, DIC2,DEC, YAD2] are used to enhance the performance of the CMOS image sensors. However, these do not increase the functionality of the imager chip [MOI].

1.3.3 Conventional vs. vision chip machine vision

The smart imagers, on the other hand, address the quality of processing the outputs from the signal processing stage by integrating algorithms to address specialized applications. They offer several advantages in terms of speed of processing, cost, size and power dissipation. Figure 1.7 shows the difference between conventional and vision chip approaches of the sensor design [PAI]. While many conventional image sensors transmit the high throughputs of raw visual data to a Digital Signal Processor (DSP) for post processing, the vision chip processes the image on chip and transmits the output (analog or digital) with a low bandwidth, providing a simplified external digital platforms.

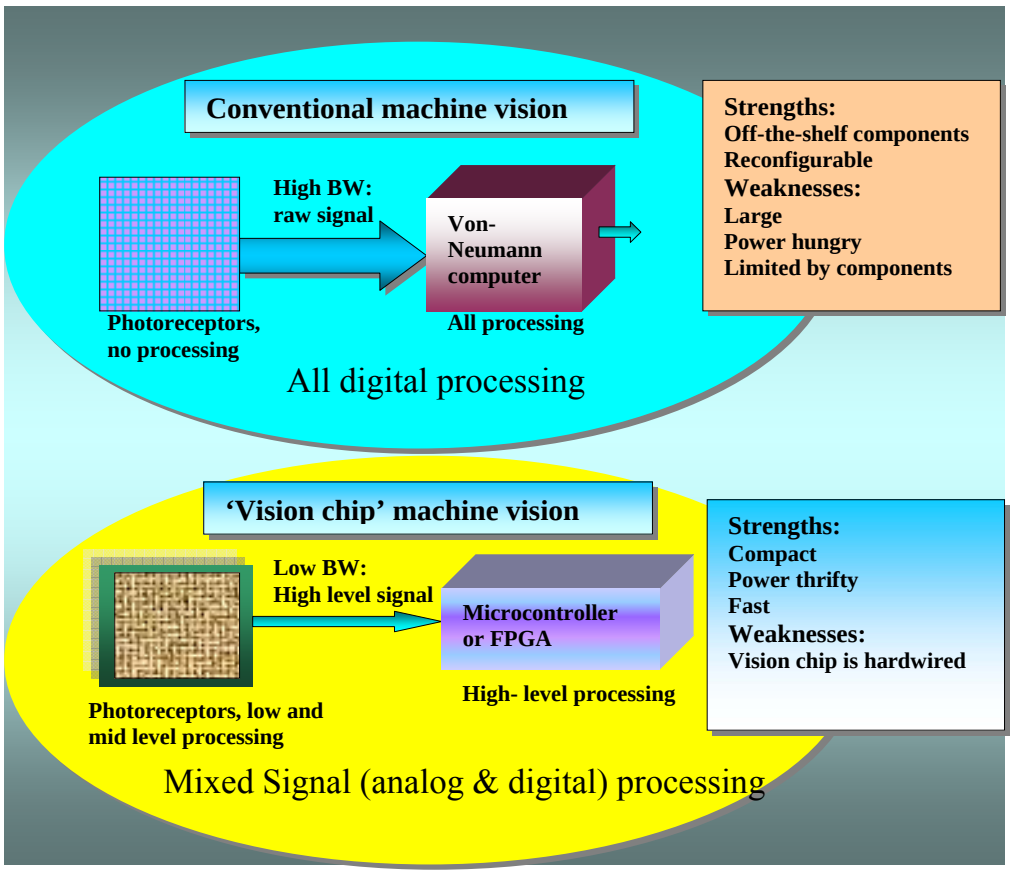

Figure 1.7: *Conventional vs. vision chip machine vision [PAI]*

To sum up the design issues of a vision chip, one should consider several issues including phototransduction to high-level image processing algorithm implementation, from analog to mixed analog / digital to digital design, from analog/digital design to digital noise techniques, from optics to electronics and optoelectronics.

For smart image sensors, CMOS technology is suitable as it enables integration of image sensing and processing logic.

1.3.2.1 Some issues on using CMOS technology for smart image sensors

Since, most of these devices need to be built from scratch due to their specialized nature, this approach is error prone and time consuming. The incorporation of extra features also may result in sacrificing some imaging characteristics, such as resolution, frame rate and power, to enhance the functionality of processing [MOI]. Also, because image-sensing is relatively a new area for CMOS, the photodetector structures are not well characterized and it is the designers' responsibility to ensure the photodetector's functionality.

1.4 Smart CMOS image sensor for 3D measurement

The objective of this thesis is to present a smart CMOS image sensor for 3D measurement applications using sheet beam method based on active triangulation. The image sensor is proposed with a 2D architecture consisting of N closely packed slices of linear sensors, working independently and in parallel. Each linear sensor, emulating a 'position sensitive device' (PSD), estimates the position of the light spot impinging on it through centroid estimation. By accumulating the centroids of all the light spots, the 2D sensor can reconstruct the profile of the object. As the functionality of linear sensor is replicated in the array in an identical way, the major discussion of the thesis is around a linear image sensor.

1.5 Salient features and scope of the work

The design addresses the 3D imaging problem through N-1D problems thus reducing design complexity. It proposes a novel position to pulse conversion mechanism for image binarization and multiple images binarization to achieve high sub-pixel resolution of position estimation. It also ensures modularity and high level of parallelism in the architecture by implementing the sensor as an array of identical slices. The device presented here is a linear smart sensor as the principle is to be proved in 1D and then extend the same to a 2D architecture.

The following section briefly discusses the organization of the thesis.

1.6 Structure of the thesis

In Chapter 2, a survey of the state of the art in CMOS imaging is presented with an emphasis on imagers used in 3D measurements in general and those using active triangulation techniques in particular.

Chapter 3 consists of the background and the basis for the thesis explaining the concepts used in designing the device. These include the stages of signal acquisition and processing, centroid algorithm, multiple images binarization, asynchronous mode of operation in position to pulse conversion and concepts of sub pixel resolution.

In Chapter 4, the design of the Smart CMOS imager is presented. Various functional blocks of the device, the implementation of the position estimation algorithm in hardware to calculate centroid of the spot, the array design and the 2D architecture are explained.

In Chapter 5, the testing and testability features of the device are explained. The electrical testing and the test setup with optical bench are discussed. Interfacing with FPGA is presented.

In Chapter 6, the analysis of test results is discussed and a comparison with the related work, mentioned in state of the art, is presented.

Chapter 7 summarizes the work of the research and presents the conclusions derived from this research along with directions for future work.

Chapter 2

State of the art in CMOS image sensors for 3D measurement

2.1 Introduction

This chapter provides a brief background on the range sensors, the triangulation method and of the CMOS based solutions to 3D measurement problems. Though not exhaustive, it covers the historical perspective of devices used in the triangulation-based measurements, viz., PSD (position sensitive device), CCD detectors and laser line devices. Subsequently it introduces the developments in CMOS imagers for the specific 3D measurement applications with a review of the state of the art sensors.

2.2 Active range imaging using optical triangulation method

The most common active triangulation methods include illumination with a spot beam and a sheet-beam. After discussing the relative merits of each scheme, this section suggests the method adapted in this thesis.

2.2.1 Principle of 3D measurement with spot beam projection method

Figure 2.1 shows the spot beam range imaging. A projected spot beam is reflected on a target object and reached on the sensor plane. Therefore, in order to obtain an *MxN* image *MxN* measurements have to be made. The range data of a target object are acquired by triangulation with the projected beam direction and the position of incident beam on the sensor plane.

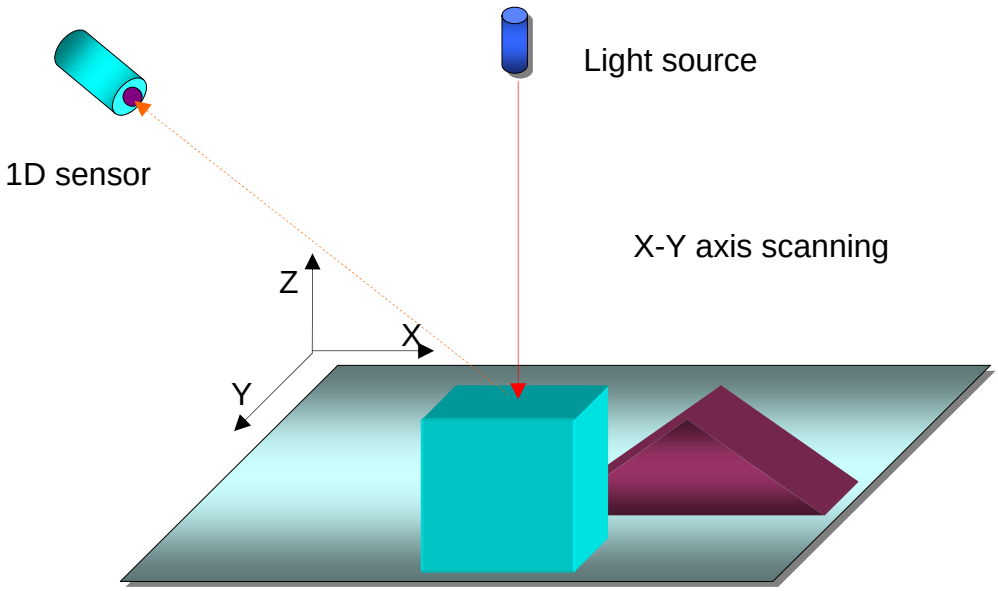

Figure 2.1: *Spot beam range imaging [IVP]*

The principle of triangulation-based range calculation is shown in Figure 2.2, in which a light source and a sensor are placed at a distance of *d*. A scanning mirror provides α_1 and θ as a direction of projected beam. θ can also be provided from the Y position of projected beam on the sensor plane. When a target object is placed at $R(X_R, Y_R, Z_R)$, the position sensor detects the reflected beam at $e(xe, ye)$.

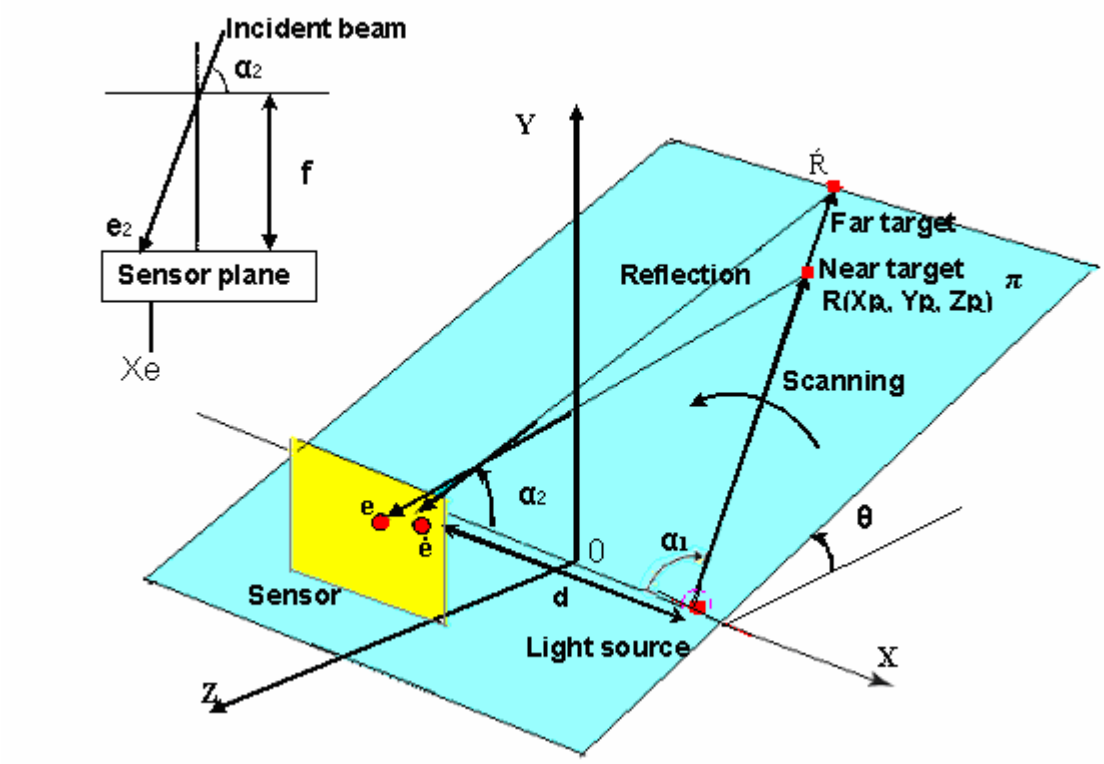

Figure 2.2: *Principle of triangulation based range calculation [OIK1]*

$\alpha 2$ and θ are given by

$$\tan\alpha_2 = \frac{f}{x_e} \quad (2.1)$$

$$\tan\theta = \frac{f}{y_e} \quad (2.2)$$

where f is focal depth of the sensor. α_1 and α_2 are given by

$$\tan\alpha_1 = \frac{l}{d/2 - x_p} \quad (2.3)$$

$$\tan\alpha_2 = \frac{l}{d/2 + x_p} \quad (2.4)$$

here l is length of a perpendicular line from R to X axis. Hence, X_R and l are given by

$$x_R = \frac{d(\tan\alpha_1 - \tan\alpha_2)}{2(\tan\alpha_1 + \tan\alpha_2)} \quad (2.5)$$

$$l = \frac{d\tan\alpha_1\tan\alpha_2}{\tan\alpha_1 + \tan\alpha_2} \quad (2.6)$$

here $Y_R = l \sin\theta$ and $Z_R = -l\cos\theta$.

$$Y_R = \frac{d \tan\alpha_1 \tan\alpha_2 \sin\theta}{\tan\alpha_1 + \tan\alpha_2} \quad (2.7)$$

$$Z_R = \frac{d \tan\alpha_1 \tan\alpha_2 \sin\theta}{\tan\alpha_1 + \tan\alpha_2} \quad (2.8)$$

The range image of the target scene can be acquired by the range calculation using whole position detection of a scanning beam.

2.2.2 Principle of 3D measurement with sheet beam projection method

In this method, a sheet beam is scanned [IVP] over the scene and one row with *N* values is acquired at each light position, as shown in Figure 2.3. Using the projected beam direction and the position of incident beam on the sensor plane, the range data of a target object are acquired by triangulation. X-axis being the scan direction, the sensor detects the centre line positions of an incident sheet beam on the sensor plane. Since the 3D measurement system with sheet beam needs just N frames, it reduces the number of required frames for a range map of position detection with N×N pixel resolution. Though it enables to realize a high-speed range finding system, more pixels are activated on the sensor plane than that of a spot-beam-projection system.

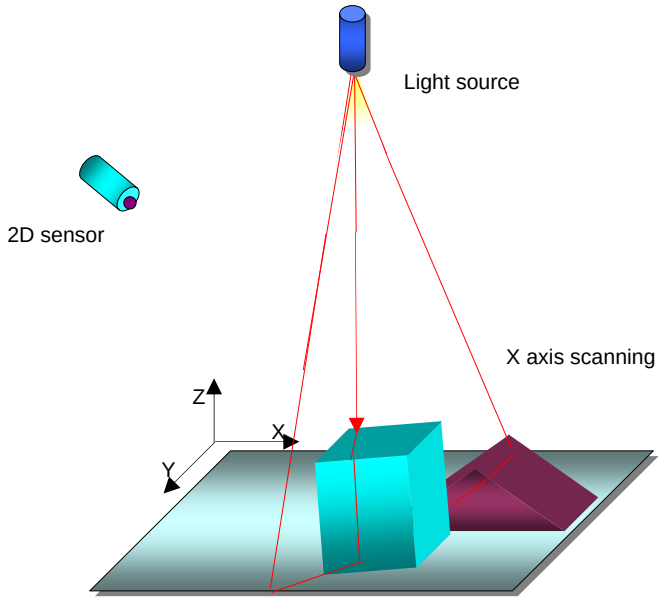

Figure 2.3: *Sheet of light range imaging [IVP]*

For each position of the sheet beam, the depth variation of the scene creates a contour, which is projected onto the sensor plane. If we extract the position of the incoming light for each sensor row, we obtain an offset data vector, or profile, that serves as input for the 3D computations.

To make a sheet beam sharp, the laser spot-light passes through a lens. The lens spreads the light into a sheet in one dimension while it is unaffected in the other. The two-dimensional range images can be obtained in three ways: by moving the apparatus over a static scene, or by moving the scene, or by sweeping the sheet beam over a static 3D-scene using a mirror arrangement. In the first two cases, the distance can be computed from the offset position in each row using a simple range equation. However, in the third

case, since the direction of the emitted sheet beam changes, a second triangulation parameter becomes involved for each light sheet position, which is not desirable.

For each illumination position and sensor integration, the output from the 2D image sensor should be reduced to a 1D array of offset values. Many commercial sheet beam range imaging systems [BLA, MAL] are based on video-standard sensors, with a preset frame-rate (50 Hz in PAL standard) limiting the range profile frequency to 50 Hz. A 512x512 range image is then obtained in 10 seconds, and the range pixel frequency is 25 kHz. Even if the frame rate could be increased, the sensor output is still serial, which would require very high output and processing clock frequencies and possibly increase the noise level [IVP].

The spot beam technique requires advanced mechanics to allow the spot to reach the whole scene. At least two synchronous scanning devices are required. The advantage is that a relatively simple linear sensor, e.g. of the position sensitive device type, can be used. However, the use of only one single sensing element often reduces the acquisition speed. In the case of sheet beam systems, the projection of the light can be done with one single scanning mirror.

The optical triangulation based on the sheet beam method is the most suitable in terms of cost, complexity and resolution for mid-range 3D measurement systems, as it offers < 1 mm range finding at a distance of several meters, and high robustness of measurement environment due to active range finding. Future 3D applications like advanced gesture recognition systems, accurate shape measurements, 3D pictures and scientific observations require the high speed and high resolution imagers [OIK1].

2.3 Range sensors

A range sensor measures the distance between a reference point and a specified target. Therefore, a *range image* is a large collection of distance measurements from a known reference coordinate system to surface points on object(s) in a scene. If *scenes* are defined as collections of physical objects then *surface points* are defined as the 3-D points [BES].

The applications of range sensors can be divided into two categories: (i) finding the distance to the closest object and (ii) determining the general shape characteristics. Whereas robot navigation and obstacle avoidance are examples of the first category, depth map applications belong to the second. Algorithms with low computational complexity can realize the distance measurements, while depth map requires that every point on the object be identified precisely to obtain the shape. Hence, most of the time, complex mathematical methods are used to realize such systems.

Sensor viewing constraints are the primary issues to be addressed in range imaging sensor requirements. In [BES], four basic types of range sensors are distinguished, based on the viewing constraints, object movement possibilities and scanning mechanisms: “

- A point sensor measures the distance to a single visible surface point from a single viewpoint along a single ray. A point sensor can create a range image if (i) the scene object(s) can be satisfactorily "scanned" in two orthogonal directions in front of the point-ranging sensor, or (ii) the point-ranging sensor can be scanned in two directions over the scene, or (iii) the scene object(s) are stepped in one direction and the point sensor is scanned in the other direction.

- A line sensor measures the distance to visible surface points that lie in a single 3-D plane that contains the single viewpoint or viewing direction (method also known as light sectioning). A line sensor can create a range image if (I) the scene object(s) can be satisfactorily "scanned" in the direction orthogonal to the sensing plane, or (2) the line ranging sensor can be scanned over the scene in the orthogonal direction.

- A field-of-view sensor measures the distance to many visible surface points that lie within a given field of view relative to a single viewpoint or viewing direction. This type of sensor creates a range image directly. No scene motion is required.

- A multiple-view sensor locates surface points relative to more than one viewpoint or viewing direction because all surface points of interest are not visible or cannot be adequately measured from a single viewpoint or viewing direction. Scene motion is not required.

These sensor types form a natural hierarchy: a point sensor may be scanned (with respect to a sensor axis) to create a line sensor, and a line sensor may be scanned (with respect to the orthogonal sensor axis) to create a field-of-view sensor. Any combination of point, line, and field-of-view sensors can be used to create a multiple-view sensor by rotating and translating the scene in front of the sensor(s)." [BES]

Range-imaging sensors are the data-gathering components of range-imaging systems, which themselves are the machine-perception components of application systems. Algorithms, software, and hardware are typically developed in isolation and brought together later, but by incorporating programmability features in hardware, (ex: vision chips) the operation of the application systems can be expedited.

2.4 Triangulation sensors: An overview

Triangles are the basis of many measurement techniques, from basic geodesic measurements performed in ancient Greece to more modern laser-based 3D cameras [BER3]. The Greek philosopher Thales (6th century BC) has been credited with the discovery of five theorems in geometry (www.britannica.com), two of which are used to solve the triangulation equations in a range camera. They state that opposite angles of intersecting straight lines are equal and a triangle is determined if its base and the angles relative to the base are given (Figure 2.4). Choosing one of the three laws, i.e. sines, cosines and tangents, solves the last theorem.

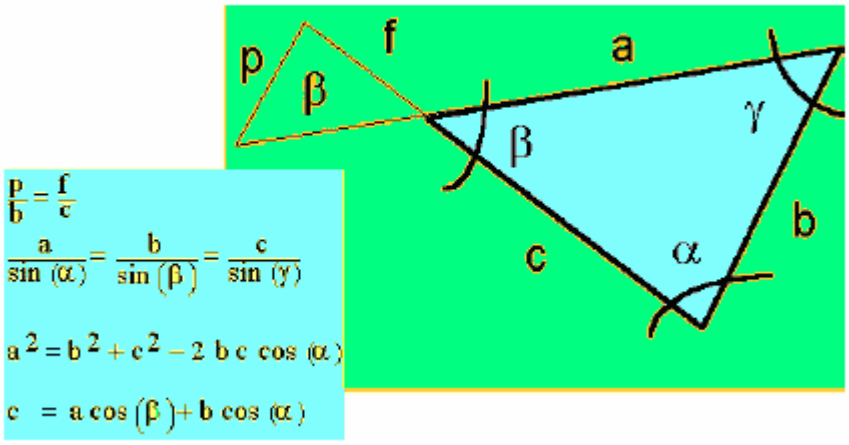

Figure 2.4: *Similar triangles and cosine law [BER3]*

While the principle of optical triangulation has been known for centuries (invented by Gemma Frisius in 1533), the use of triangulation for automated measurement is a relatively new technology. This is not because of knowledge of how to make a sensor but rather because of availability of suitable components. During the 70's the practical triangulation sensors for industrial applications have started becoming available, enabled by the commercialization of solid-state detectors and early microcomputers.

Triangulation sensors are widely used for inspection of dynamic materials [PAS], such as monitoring tyre dimensions while rotating at high-speed, closed loop control of pouring of molten metal and 3D contouring profiles of logs and boards. Laser triangulation sensors are also ideal for monitoring vibrations, without adding the mass of a sensor to a component, which would alter the vibration characteristics of the object.

The triangulation sensors generally use light source of relatively high intensity, such as laser. Since triangulation requires finding the location of the centre of the imaged spot, the imaging detector must be capable of detecting the spot location. Traditionally, there are two types of solid-state detectors: position sensitive device (PSD) detector and the charge coupled device (CCD) detector.

2.4.1 PSD Detectors

The PSD is an analog detector [PAS], which relies on the current generated in a photodiode and converts incident light into continuous position data, with outputs at both ends, A1 and A2. The output current is proportional to the reflected light spot's position on the detector. If the reflected light is in the middle of the detector, the analog outputs at each end are equal, but as the light moves from the centre of the detector, the outputs change proportionally. The receiving element finds the position of the centre of the average light quantity distribution. There is no other information that the PSD element can provide.

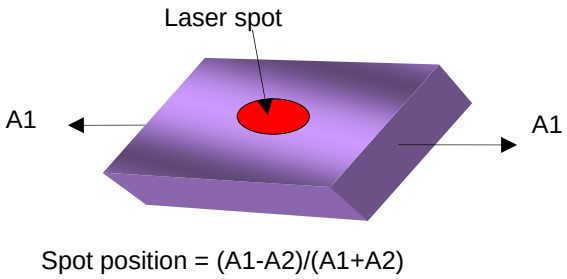

Figure 2.4: *Position sensitive detector*

Disadvantages of the PSD include lack of ability to display an image or profile of the detector pattern. Also, the PSD determines the centre of all light that falls on the detector area. If more than one spot or other light falls on the detector, it will report the position of the centre of all light, as if the center of gravity of the light spot is shifted, possibly giving an erroneous signal. Another consideration is that PSD systems are sensitive to light intensity. This is inherent in the detector. If the light intensity changes and the spot position remains the same, the output changes. This is the net effect when the target's colour changes.

2.4.2 CCD Detectors

A CCD is basically an array of closely spaced MOS diodes, in which the light is recorded as an electric charge in each diode. Under the application of a proper sequence of clock voltage pulses, the accumulated charges can be transferred in a controlled manner across the semiconductor surface to the output of the device. The output contains information on the light quantity distribution all over the active area. In the point triangulation sensors [PAS], a single dimension CCD is used, as shown in Figure 2.5.

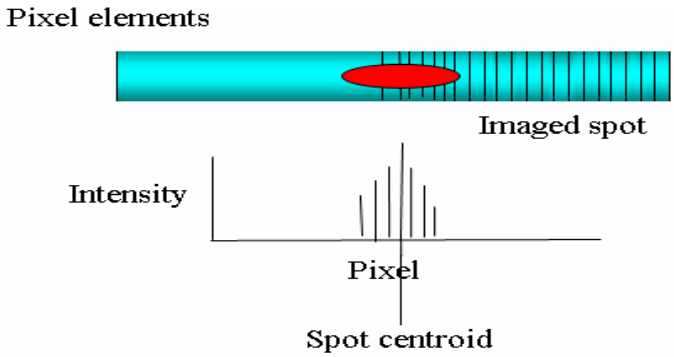

Figure 2.5: *CCD detector*

Figure 2.6 illustrates the light intensity distribution and position detection with a CCD element and an analog PSD element. Colour changes and stray reflections result in position-detection errors when a PSD element is used. On the other hand, the CCD element gives the exact position regardless of target colour, tilt, or stray reflections. Disadvantages of the CCD detector are related to speed of operation, which typically is less than that can be achieved with a PSD. Gain control in CCD based sensors is not as fast as in PSD based sensors, a drawback in applications where surface reflectivity changes rapidly.

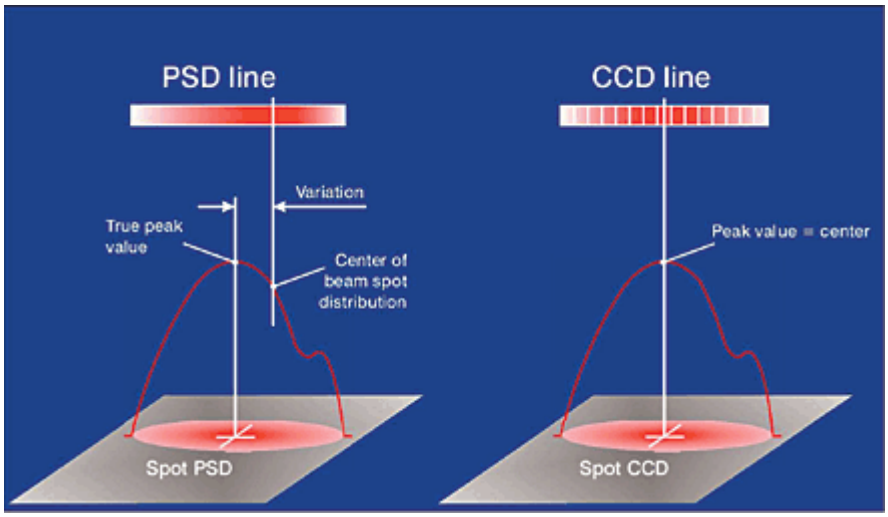

Figure 2.6: *PSD vs. CCD [DUM]*

2.4.3 Laser line sensors

A better version of the CCD based detector is commercially available (ex: L1 sensor family- LMI Inc.)

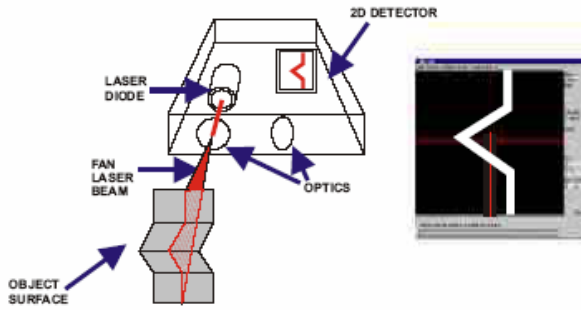

Figure 2.6: *Laser line sensor [PAS]*

Using a 2D CCD as the detector, this sensor collects multiple points in a frame generating the contour of the surface, as shown in the Figure 2.6. If the part is moving under the sensor, a 3D map of the surface can be generated.

However, this approach is slower in data acquisition rate than a single point triangulation sensor, and typically provides medium accuracy specifications. It also requires that part surfaces be reasonably uniform in reflectivity, since gain control can only be provided over the full field of view.

This discussion points out that these sensors are not suitable for real time 3D measurement applications, where speed and high accuracy of position estimation are both important. The following discussion briefly gives the state of the art in CMOS imagers for 3D applications with active triangulation as the method of measurement.

2.5 Image sensors for 3D measurement

3D measurements are concerned with acquiring geometrical shape of the object in contrast with the 2D imaging, where only local reflectivity is the matter of concern. The vision sensors used for the 3D imaging applications may consist of CCD or CMOS image sensors / processors, which in turn may be made of arrays of pixels, or columns or processor cores with processing elements (also known as vision system on chip VSOC). The output often is not images but information for decision-making. Several factors are to be considered for the design of a 3D imager to work in real time. The design of the chip can take any of the following forms:

(i) Chip level processing: where a processor core (mostly off-the-shelf) and sensing elements are interfaced in a single casing for performing vision tasks
(ii) Column level processing: where one processing element for each column of the array is used for undertaking local processing, and
(iii) Pixel level processing: where each pixel in the array contains its own processing element.

[PAI] illustrates the approaches of VSOC and the related advantages and disadvantages.

Table 2.1: *Vision system on chip: comparison of processing*

	Advantages	**Drawbacks**
Chip level processing (CHLP)	Versatile, flexible, compact, good resolution achievable with small pixel size, simple programming model, standard image processing algorithms, Easy IP block combining, small pixel and array sizes etc.,	Low performance / speed. Performance decreases quadratically as array size grows. Does not allow close sensor-processing retroaction.
Column level processing (COLP)	Good processing speed, better frame rate / readout speed, small pixel, high resolution.	Performance decreases linearly as array size grows. Processing performance depends upon chip orientation. Algorithms are to be thought differently.
Pixel level processing	Very high processing speed. Best frame rate / readout. High speed achievable, close sensor-processing retroaction possible.	Large pixel size / small array size. Algorithms are to be totally rethought

Table 2.2 shows the merits of single chip integration single chip vs. separate chips for sensor and processing. Though the comparisons in the reference are mainly with reference to VSOCs, they also are applicable to the vision chips used in 3D measurements.

Table 2.2: *Single chip integration vs. separate sensor / processing*

Criteria	**Single chip integration**	**Separate chips for sensor and processing**
Power	(+) Only minimum hardware integrated. No inter-chip communication which wastes power, optimal use of parallelism / low frequency requirement, low voltage	(-) General purpose chips, involving unnecessary functionalities, energy wastage, high frequency needed, high power chip-to-chip communication: wastes energy
performance	(+) Parallelism integrated at pixel level, high speed, high frame rate	(-) High latency data access, sensor to processing chip bottleneck
Accuracy	(-) Sensing / processing quality trade-off	(+) Sensor chip only, so no processing noise, optimised for best sensitivity / accuracy
Volume / size	(+) Single chip : most compact	(-) Few chips
cost	(+) Single chip, standard CMOS process	(-) Costly CCD process, multiple chips, casing and board integration

(+) advantage and (-) drawback

Most smart sensors cited in the literature, follow the pixel level processing and are implemented as single chip solutions. The following discussion presents analysis of the state of the art smart imagers for 3D measurement using triangulation methods.

2.6 State of the art smart sensors for 3D measurement using active triangulation

Almost all the 3D measurement applications, in the present context, rely on the accurate computation of the centroid. Low power, high-speed, accurate computation of centroid in the image plane is also important for many applications including: object tracking in robotic systems [BER2], autonomous navigation [ZUF], space guidance and navigation systems [SCH2], and deep-space optical communication systems [ALE] that require accurate and stable beam pointing for high speed data transfer. Off-focal-plane digital processors yield accurate centroid values, but only at the cost of increased latency, power and size [PIE]. On or near focal plane centroid computation using current mode circuits and neuro-MOS circuits have been implemented [DEW]. However, neither approaches are integrated with high performance image sensors, nor are they entirely compatible with one [SUN].

A range finding chip [GRU] with cell parallel architecture is proposed for parallel sheet beam range detection. When the beam passes over a photodetector, a current pulse is generated. The position of the pulse, in time, gives a measure of the range. It is reported that 1000 frames per second is achieved with 0.5 mm accuracy. However, this falls short of the real time 3D requirement in terms of frame rate and accuracy.

The commercial photodiode arrays, often used in 3D vision sensors, are intended for 2D imaging applications, where the specifications change according to the evolution of their respective fields and not related to digital 3D imaging. For example, speckle noise dictates a large pixel size [BAR] that is not compatible with current 2D imaging developments (where pixels are getting smaller). Many devices have been built or considered in the past for measuring the position of a laser spot, viz., continuous response position sensitive detector (CRPSD) and discrete response position sensitive detector (DRPSD) [MAY]. While a CRPSD provides the centroid information in continuous mode, very precisely, a DRPSD (detectors implemented in CCD or CMOS), on the other hand, provides information relative to the spot position with a higher accuracy, but is slower [BER4]. Since accuracy is more important than precision, a DRPSD is generally preferred. An integrated approach combining CRPSD and DRPSD [SIM] is proposed for achieving good precision with high accuracy. However, these cannot integrate smart features and hence not efficient in terms of quality of image processing nor can achieve the speeds anticipated for real time needs.

A high speed position sensitive detector is reported in [MAS], employing analog intensive parallel computation for the estimation of the position of the centroid of the light spot. The centroid detection algorithm is based on binarization. Though this device cannot be compared with a 3D measurement application, the algorithm implemented in this thesis has roots in this design. However, the similarity ends there.

The central nervous system uses asynchronous pulse coding to share the results among neurons in the brain [KOC]. It will be interesting to investigate if this strategy can be used in the vision chips. The output of any photoreceptor array is usually scanned serially and the entire image is read out for processing, no matter whether anything of interest happened in the interval. Thus, each pixel in the image gets a fixed fraction of the total communication and processing bandwidth. However, this will be a waste of bandwidth. A more intelligent strategy would be to send out a signal only when an event has occurred, as that happens in most parts of the brain. Multi-chip systems based on such asynchronous communication protocols have been designed by a number of researchers [AND, BOH, CUL, LAZ, SHI, VIT], to name a few. Individual pixels generate a pulse (or spike, in the language of neurobiology) that is assigned a unique address and placed on a bus. The chip that receives the retina output then knows that something of interest has happened at that address.

There is a similarity between this thesis and the references cited here as far as the concept of asynchronicity and pulse based approach is concerned. However, this thesis does not have any leaning towards biological inspiration, nor contains concepts of analog neural processors. Nevertheless, the advantage of using spikes or pulses is explored in the device design.

Some conventional high-speed position sensors have been reported in [BRA1, BRA2, BAK, YOS, SUG] which are developed for range finding, based on the sheet beam method. A computational sensor is proposed in [BRA1] to increase the process speed by selecting the sub-regions of the image that require processing, pre-process them and transmit the data only from the sub-regions. The sensor uses a row-parallel winner-take-all (WTA) circuit and can acquire a 64×64 range map in 100 range maps/s. However, the pixel resolution is limited by the precision of the current mode WTA circuit. Thus, it is difficult to realize this sensor for real time range finding with high pixel resolution.

The sensor using pixel-parallel architecture [YOS] achieves 192×124 range finding in video rate. It has a large pixel circuit for frame memories and an ADC. To reduce the pixel size, a 320×240 (QVGA) colour imager is developed with analog frame memories [SUG]. Though it makes a pixel circuit smaller and realizes 160×120 3D imaging in 15 range maps/s, the range finding rate is inferior to [YOS]. Hence, it is also difficult to get a 3D image in real time with higher pixel resolution.

A position detection sensor for 3D measurement, reducing the number of cycles for position detection is reported in [NEZ1], when activated pixels exist locally on the sensor plane. The operation cycles are given as $O(\log_2 N)$ theoretically. In [NEZ2], which has a row parallel sensor architecture, it is reported that the sensor is suitable for a range finding system with sheet beam projection and can achieve real time

operation with 75 range maps/s at 0.5 sub-pixel resolution. The device proposed in this thesis projects the order of range maps suitable for 3D measurement along with high sub- pixel resolution.

In [OIK1], a high-speed position sensor using quad-tree scan is introduced, which has the capability of 10k points/s position detection of a projected spot beam. Three other position sensors for a high speed range finding system with sheet beam projection are reported, which include two row-parallel architectures for quick position detection on the sensor plane and a real-time 3-D image sensor with high pixel resolution is presented. It employs a high-speed readout scheme with adaptive threshold circuits, which allows a compact pixel circuit implementation for over-VGA pixel resolution. [OIK2] presents an improved version of the chip mentioned in [OIK1]. Though no claim is made in this thesis on surpassing these chips, by careful observation it will be apparent that the design used in this thesis is much simpler and has some unique approaches in the architecture implementation.

2.7 Conclusions

In this chapter, spot beam and sheet beam based triangulation methods are described. The characteristics of range sensors are discussed. For historical perspective, triangulation sensors comprising PSD, and CCD detectors and commercial laser line sensors are introduced to underline the evolution of the position detection sensors. For 3D measurements in real time, these devices are not used as they do not match the speed and resolution criteria. The vision processing methods are compared and the advantages of single chip vs. multi chip approach are briefly discussed. The need for dedicated vision chip for performing specific task is highlighted, paving way for the smart sensor design. State of the art smart imagers are reviewed in order to compare the design presented in this thesis. A comparative chart will be presented in the results and analysis chapter to compare the salient features of various designs.

Chapter 3

The Background

3.1 Introduction

This chapter introduces the concepts behind the design of the vision sensor in the context of sheet beam based 3D measurement using active triangulation methods. The design involves addressing wide ranging issues from implementing a suitable visual processing algorithm in CMOS VLSI for the 3D measurements on one end (at the highest level) to acquiring the image information by a photoreceptor on the other end (at the lowest level).

In the following sections, the design criteria are discussed. The chapter on Sensor design is based on these foundations. Subsequently, pixel level processing and image binarization with non-conventional A/D conversion are discussed. The advantages of this early digital approach are highlighted.

3.2 Design criteria and guidelines

Pixel is the basic building block of a vision sensor, which carries out the phototransduction to process the incident light from the scene into a measurable electrical signal. The output of the pixel is then processed in order to interpret the scene characteristics. In addition to the photodetecting and image acquisition circuits, a vision chip requires analog conditioning and processing circuits, digital processing and interfacing, and image readout circuitry all on the same chip. The vision chip may contain several (order of hundreds) arrays of the photodetectors along with the processing circuits. In most cases of the imager implementations, these components should interact with at least their nearest neighbours. This involves a close interaction of the optoelectronics, and electronics parts of the device, which contains photodetectors, analog, digital and mixed mode elements. Additionally, a vision chip for 3D measurement has to implement the visual processing algorithm of the imaging task.

To design a vision sensor for 3D measurement, in this context, one has to consider several issues: how soon the incident light, converted in to analog voltage by the photodetector, can be transformed into digital domain for efficient data processing; what should be the form of the output data; how efficiently the data can be handled; how to implement the search algorithm on the focal plane of the device to detect the centroid of the light spot precisely; how to process the data and output the same to further stages of the image processing chain; and finally how to interpret the output data.

The use of pulses for computation has good potential [WAT] in the circuit design. Circuit implementations using continuous analog signals are subject to noise and will be especially problematic when the signals must be communicated across the chip boundaries. A pulse-coded process can use a single wire for communication like analog voltages and currents, but retains noise immunity of digital signals. Using simple digital techniques, binary pulses can be buffered and transmitted without loss of performance. Pulse based approach can effectively exploit the best features of both analog and digital circuits.

Secondly aiming at high modularity and parallelism in the design by means of pixel and column level processing, the architecture becomes reusable, replicable and trouble shooting can be easier. These are discussed in the chapters on design and testing.

Keeping the above mentioned issues in view in the design of the vision sensor, the following parameters have been considered:

- Transform the analog photo signal into digital at the earliest in the image processing cycle
- Interpret the position of the pixel in pulses and binarize the information
- Implement the centroiding algorithm for identifying the position of the light spot
- Achieve high modularity and parallelism in the architecture,
- Combining the processing of pixel level and column level architectures to take advantage of both the domains in terms of speed and resolution and
- Process the sensory information serially in the array and in parallel at the sensor level

The following sections discuss on the issues presented here.

3.2.1 Photodiodes in standard CMOS process

A p-n junction diode is a CMOS compatible device, which can be used as photodetector in image sensors. In a standard CMOS process, several structures can be formed to convert light into an electrical signal. These structures, which are mainly junction devices, are shown in Figure 3.1 for an n-well process (the complementary structures are obtained in a p-well process).

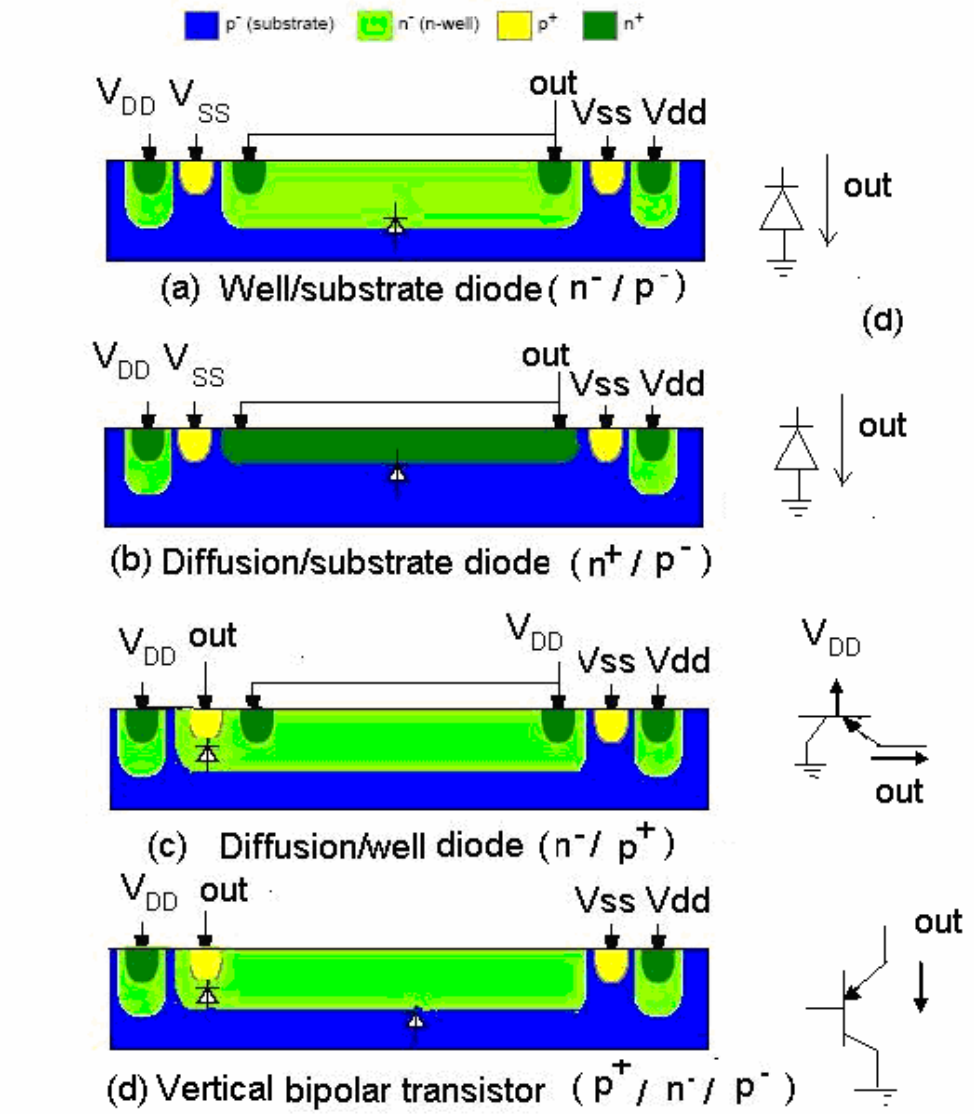

Figure 3.1: *Junction devices available in a standard n-well CMOS process for light detection*

The first three structures are p/n junction diodes, whereas the last one is a vertical bipolar junction transistor (BJT). A diode is formed by well/substrate (n^-/p^-) junction, as shown in Figure 3.1(a), or source-drain diffusion/substrate (n^+/p^-) junction, as shown in Figure 3.1(b), or source-drain diffusion/well (p^+, n^-) junction, as shown in Figure 3.1(c)). Vertical p/n/p bipolar junction transistor is obtained by the structure formed by source-drain diffusion, an n^- well and the p^- substrate, as shown in Figure 3.1(d).

3.2.2 Phototransduction and response [ELE]

The detected signal in a photodiode can be represented by a photogenerated current [SZE1]:

$$I_{ph} = \frac{q.A : P.\lambda.\eta}{h.c} \tag{3.1}$$

where q is the electronic charge, A is the detector area, P the incident light power per unit area, λ the wavelength of the incident light, h the Planck constant, c the speed of light in vacuum and η the absolute quantum efficiency of the process at wavelength λ . Here, η is defined as the number of electrical charges detected per incident photon,

$$\eta = \frac{\text{number of detected charges}}{\text{number of incident photons}} \tag{3.2}$$

The quantum efficiency is specific to each photosensitive device and is a function of the wavelength of the incident radiation. One of the factors that determines quantum efficiency is the absorption coefficient α, which is a strong function of the wavelength of the incident light. For silicon, the absorption length, $L(\lambda)$, which is the inverse of the absorption coefficient ($L(\lambda) = 1/\alpha$). For a given semiconductor, the long cut-off wavelength, λ_c, is determined by the energy gap of the material, Eg. For silicon Eg = 1.12eV, which corresponds to λ_c =1.1 μm according to the relationship:

$$E = \frac{hc}{\lambda} = \frac{1.24}{\lambda} \quad \text{(eV.μm)} \tag{3.3}$$

where E is the photon energy.

For an abrupt junction diode, the width of the depletion region is given by [MUL]:

$$W = \sqrt{2\frac{\varepsilon s}{q}\left(\frac{1}{Na} + \frac{1}{Nd}\right)(\phi_{bi} + Vr_{es})} \tag{3.4}$$

where ε_s is the permittivity of silicon, φ_{bi} the built-in potential of the junction, V_{res} the reverse applied voltage, N_d the donor concentration in the n-type silicon and N_a the acceptor concentration in the p-type silicon. As can be seen from Equation, the depletion region width is a function of the square root of the reverse applied voltage to the diode. Therefore, by increasing the reverse bias, there will be an improvement in the response of the detector. The depletion region width can also be increased by reducing the doping levels, although this is not possible in a standard CMOS process. However, it is expected that those diodes formed by the least doped materials will present a higher response.

3.2.2.1 Spectral Response

The spectral response of the diode is a measure of the photocurrent generated *per* incident photon with light wavelength. The spectral response of the three different diodes available in a standard CMOS process is mainly determined by the absorption of light in silicon, which is wavelength dependent. This dependency causes photodetectors formed with junctions of different junction depths to have different spectral responses.

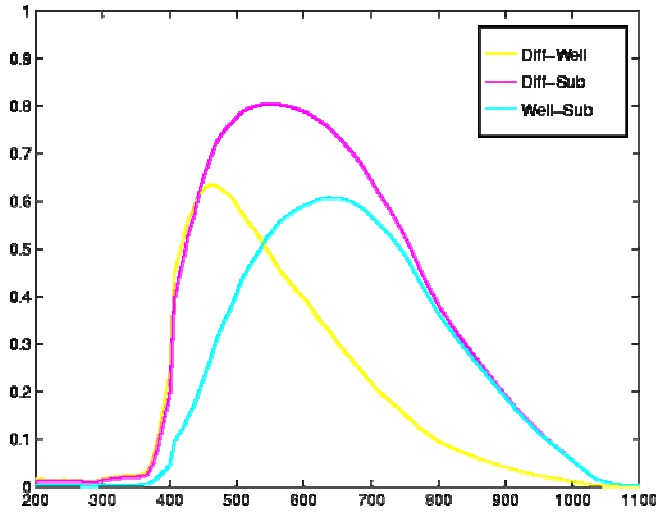

Figure 3.3: *Simulated quantum efficiency versus wavelength for three different junction diodes in a 2 µm process [MOI]*

The (n^-/p^-) and (n^+/p^-) diodes behave similarly. The (p^+/n^-) diodes are more sensitive at shorter wavelengths [DEL] [SON]. According to their spectral response, the (n^-/p^-) and (n^+/p^-) diodes are better suited for imaging applications since their quantum efficiency is higher in the visible spectrum. Besides, these two structures need smaller processing areas compared to (p^+/n^-) diodes.

3.2.2.2 Optical Dynamic Range

The optical dynamic range of a photodiode is normally defined as the range of incident light power over which the detected signal behaves as a linear function, according to Equation (3.1). Usually its lower limit is determined by the dark current of the detector whereas the upper limit may be device or external circuit limited. Optimized photodiodes used for calibration of incident light can show very large dynamic ranges. However, for the detectors available in a standard CMOS process, which are restricted to fixed processing parameters, this range is reduced to about 5 to 7 decades of incident light intensity [MAN]. In addition, this optical dynamic range normally degrades when the detectors are coupled to signal processing circuitry. However, it can be improved by cooling the devices, since the dark current decreases when the operating temperature is decreased (as it will be seen in the next section).

3.2.2.3 Junction leakage current or dark current

As mentioned above, the junction leakage current or dark current limits the detection capabilities of photodiodes. Junction leakage current is a function of temperature and of the doping characteristics of the photodiode. Assuming a short base diode model [MUL], because of the long recombination times in a standard CMOS process, the reverse bias current can be predicted by

$$I_{reverse} = Aqn_i^2\left(\frac{D_p}{N_d W_B} + \frac{D_n}{N_a W_E}\right)\left(1 - e^{-\frac{qVres}{kT}}\right) \qquad (3.5)$$

where V_{res} is the reverse bias applied to the junction, A is the area of the diode, n_i is the intrinsic carrier concentration of silicon, D_p is the diffusion constant of holes, W_B is the distance, in the n-type silicon, between the depletion region and an ohmic region, Dn is the diffusion constant of electrons, W_E is the distance, in the p-type silicon, between the depletion region and an ohmic contact, k is the Boltzmann constant and T is the absolute temperature. The diffusion constants decrease approximately as $T^{-1.4}$ [MUL], but the intrinsic carrier concentration increases as $T3^{/2}e^{1/T}$ [MUL]. Therefore, the reverse current doubles as T increases. By controlling the fabrication process and operating the sensor at low temperatures, it is possible to reduce significantly the dark current. However, process parameters cannot be controlled in a

standard CMOS process, as they are fixed by the foundry. Therefore, the only way to reduce the dark current is by cooling the detector. It is also known that the dark current is a function of the reverse bias applied to the junction [MUL]. When the reverse bias increases (stronger reverse polarization), the dark current also increases, degrading the dynamic range of the photodetector [ELE].

3.2.2.4 Sources of noise in photodiodes

In addition to the dark current, there exist other sources of noise in photodiodes. Shot noise is caused by three different random processes: the emission of photons from a light source, which causes the photogenerated signal to be a random variable in time, the emission of carriers over the potential barrier formed in a reverse biased photodiode, which causes the dark current to be a random current, and the background radiation which produces a random photogenerated current, I_B. The noise signal due to shot noise is proportional to the square root of $(I_{ph}+I_{dark}+I_B)$.

Fixed pattern noise is defined as the photoresponse variation between adjacent photodiodes. This variation generally arises because of non-uniformities in the size and spacing between detectors in an array. The magnitude of this noise is usually less than 1% for photodiodes in standard CMOS processes.

3.2.2.5 Capacitance of the depletion region

A diode under reverse bias shows a voltage-dependent capacitance caused by the variation in stored charge at the junction. An abrupt junction diode has a capacitance given by [MUL]:

$$Cj = \frac{A}{2}\left[\frac{[2q\varepsilon_s]}{(\phi_{bi}+Vres)}\left(\frac{N_d N_a}{N_d+N_a}\right)\right]^{\frac{1}{2}} \tag{3.6}$$

where A is the junction area. To avoid large RC time constants when using external resistance loads, it should be necessary to decrease the value of the capacitance. According to equation (3.6), this can be achieved by reducing the diode area, reducing the doping level of the less doped material (Nd for a p+/n junction and Na for a p/n+ junction) or increasing the reverse bias voltage. However, each of these solutions presents difficulties for application in vision chips. A reduction in the diode area will reduce the photogenerated current, as can be seen in equation (3.1), making necessary the use of adaptation circuitry to increase the current level to that used by the signal processing circuitry. A reduction in the doping level is not possible as vision chips are fabricated in standard CMOS processes. An increase in the reverse bias will cause the depletion width to increase, therefore increasing the drift time of carriers through the depletion region [ELE].

(n^-/p^-) diode offers the lowest junction capacitance since the doping levels of this structure are lower than for the other diodes. Comparing (n^+/p^-) and (p^+/n^-) diodes, the latter ones have larger junction capacitances. In any case, for any type of diode, reverse bias should be kept not too high to avoid an increase in the drift time of carriers through the depletion region [ELE].

3.2.3 Photodiode modes of operation

The photodiodes can be operated in three basic modes:

(i) Photovoltaic mode, in which no bias voltage is applied((junction built-in potential is exploited);
(ii) Photoconductive mode, in which reverse bias voltage is applied.
(iii) Integrating mode or storage mode is a special case of photoconductive mode, in which the photodiode is initially reverse biased and then left floating, making the photo charge integrated on its capacitance.

While the first two modes of operation are characterised by a continuous sensing of the photo current, the third one provides a time-discrete output voltage which is proportional to the photo generated charge integrated over the sampling period.

The photovoltaic mode is useful if the optical power is high and the response speed is not a major concern. This mode is preferred in industrial environments, where noise problems severely affect the bias voltages. The photoconductive mode is widely used in the applications involving high speed and high optical power. The storage mode is useful for those applications with weak optical signals and for synchronising with optical sources like pulsed laser, used in active 3D measurement methods [STO].

3.2.3.1 Storage mode of operation

Also known as integrating mode, by initially reverse biasing the photodiode at a reverse voltage Vres and then leaving it floating, makes the photo charge to be integrated onto the photodiode capacitance. This mode provides a time-discrete output voltage, which is proportional to the photo generated charge integrated over the sampling period.

3.2.3.1.1 Photodiode equivalent circuit

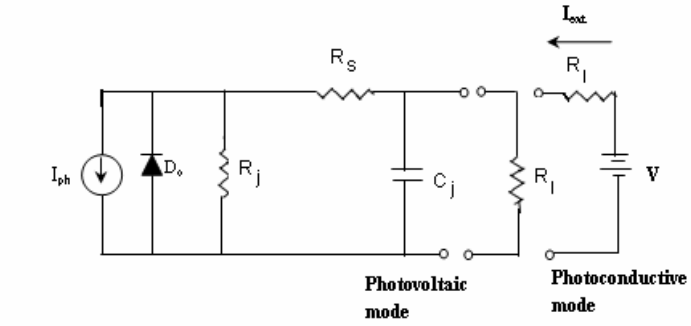

Figure3.4: *Equivalent circuit of a photodiode*

In the equivalent circuit, as shown in Figure 3.3, for photoconductive and photovoltaic modes, I_{ph} is the photocurrent, D_0 is a diode, R_s is the series resistance, R_j is the junction resistance, C_j is the junction capacitance, R_l is the load resistance, I_{ext} is the current collected by terminals and V is the reverse bias voltage.

If the incident light power is P_{ph}, the photocurrent corresponding to the current source in Figure3.4 is

$$I_{ph} = \frac{q\eta P_{ph}}{h\omega} \tag{3.7}$$

where η is the quantum efficiency of the photodiode and ω is the angular frequency of the incident light.

The responsivity R of a photodetector is defined as the ratio of induced current density to optical power density:

$$\Re = \frac{J_{ph}}{P_{ph}'} \tag{3.7.1}$$

Where J_{ph} is the light induced current density and p_{ph}' is the optical power per unit area of the incident light. The quantum efficiency is defined as the number of photogenerated carriers per incident photon:

$$\eta = \frac{J_{ph}/q}{P_{ph}'/h\omega} = R_{ph}\frac{h\omega}{q} \tag{3.8}$$

3.2.2.1 Dark current

In a reverse biased diode, a current flows also in the absence of optical generation, as a result of thermal generation processes in the bulk and at the surface. This is due to so-called dark current, which is composed of the diode leakage current, as predicted by the ideal-diode equation, and current generated in the diode space-charge region. The photocurrent and generation recombination current are indistinguishable, therefore, the magnitude of the dark current places a lower limit on the detectable light level.

The density of recombination centres is higher at the semiconductor surface; therefore, the surface space-charge region can contribute significantly to the reverse-diode current, and, hence, should be reduced in width. Further, the diode should be shaped to minimize the perimeter-to area ratio. A further important consideration is that the dark-current doubles for every 8^{o}C increase in temperature. Consequently, in a practical device, where the junction temperature is higher than the ambient temperature, dark current can limit the pixel sensitivity.

In conclusion, dark current is the fundamental limit to the sensitivity of a CMOS sensor-chip and, therefore, needs to be reduced as much as possible. A number of techniques have been suggested. Firstly, power consumption should be carefully controlled to prevent an increase in operation temperature. Further, care must be taken to ensure that the power dissipation is spread evenly across the chip, so significant temperature gradients do not exist.

3.2.4 Integration

In the storage mode of operation, the voltage drop on the photodiode decreases due to photogenerated current flowing into its terminals. Typically, this current could reach 100 fA for a pixel of 100 μm^2. A current of a few fA is difficult to detect, therefore, signal gain must be applied at the pixel site. The most common method of increasing the pixel output signal is to use an integration mode of operation [WEC]. At the start of the integration period, the pixel is reset to V_{res} by the access transistor, which is then turned off isolating the pixel. [MAR] The pixel remains isolated for the integration period during which the photocurrent discharges the pixel capacitance to produce an output signal; this is either the drop in pixel voltage or the charge removed from the pixel capacitance.

The charge removed from the pixel is simply the integral of the diode reverse current over the integration time, t_{int}. Under uniform illumination, the signal charge, Q, is given by

$$Q = \int_0^{t_{\text{int}}} i_r dt \tag{3.9}$$

where i_r is the sum of the photocurrent and reverse-diode current. It can be seen that the signal charge is linearly proportional to i_r and the integration time, t_{int}.

A significant proportion of the pixel capacitance is the voltage-dependent diffusion capacitance. Hence, while the signal charge is linearly proportional to the photocurrent, the signal voltage is not. Under the assumption of a linear diode junction, the pixel voltage, V_{pix}, is given by

$$V_{pix}(t) = \left[V_{res}^{\frac{2}{3}} - \frac{2}{3} j_{photo} \left(\frac{12}{qa\varepsilon^2}\right)^{\frac{1}{3}} t \right]^{\frac{3}{2}} \tag{3.9.1}$$

where j_{photo} is the average photocurrent *per* unit area; a is the junction doping profile gradient.

Assuming a small photodiode voltage drop, the relationship between photo generated charge and voltage drop is linear in first approximation [WEC].

3.3 The Position detection

A method of position detection is required for estimating the centroid of the light spot impinging on the imager. This section highlights the theory and implementation details of the position detection algorithm.

3.3.1 Light spot distribution

The algorithm assumes a reflected light spot with Gaussian distribution impinging on the sensor, in this case a linear array. As explained in the previous chapter, when we extend the architecture to 2D with an ensemble of linear arrays, we see that the sheet of light approach is the natural extension of the light spot approach on a linear array for the transition from position detection to finding out range maps. The light line profile reflected by the scene is 'seen' by the N linear sensors as N light spots, each impinging onto one linear sensor. Under realistic settings, each of these light spots, even though centred on a specific pixel, is spread over several neighbouring pixels with a Gaussian distribution, as shown in Figure 3.5.

For simplicity, the light spot is assumed to remain Gaussian even after reflection by the target. This is true as long as the photosensitive area of each pixel is large enough to account for speckle effects. The position of the sheet beam can then be estimated by computing the position of the N centroids of the linear sensors using multiple thresholding technique [MAS] based on the position detection algorithm, as explained below.

3.4.2 The position detection algorithm [GOT]

The algorithm integrated at array level uses multiple images binarization for the light spot position estimation. The final result is reached by sequentially processing the pixels. This solution is mainly chosen to optimize the silicon area and to realize a linear sensor suitable to be replicated in order to obtain a compact 2D sensor for range finding.

The following assumptions have been made for the sake of simplicity, which, however, do not affect the general rules of the problem:

(i) The light spot impinging on the sensor has a Gaussian shape;

(ii) The speed of the light- spot is negligible with respect to the range maps speed of the sensor. It can be supposed that the spot doesn't move;

(iii) The signal processing time is fast with respect to the evolution of the optical signal;

(iv) That there are (M+1) pixels in the array with the centre pixel number is zero, which is at the origin.

From (i), the optical power density per length impinging on the sensor can be expressed in a discrete form as:

$$p(k) = p_0 e^{-\frac{(kT - x_m)^2}{2\sigma^2}} \quad ; -M/2 \le k \le M/2 \tag{3.10}$$

where T is the pixel pitch, x_m is the centre of the function, σ is a parameter related to the width of the spot and *k* is the generic pixel of the linear sensor considering the reference system of Figure 3.5.

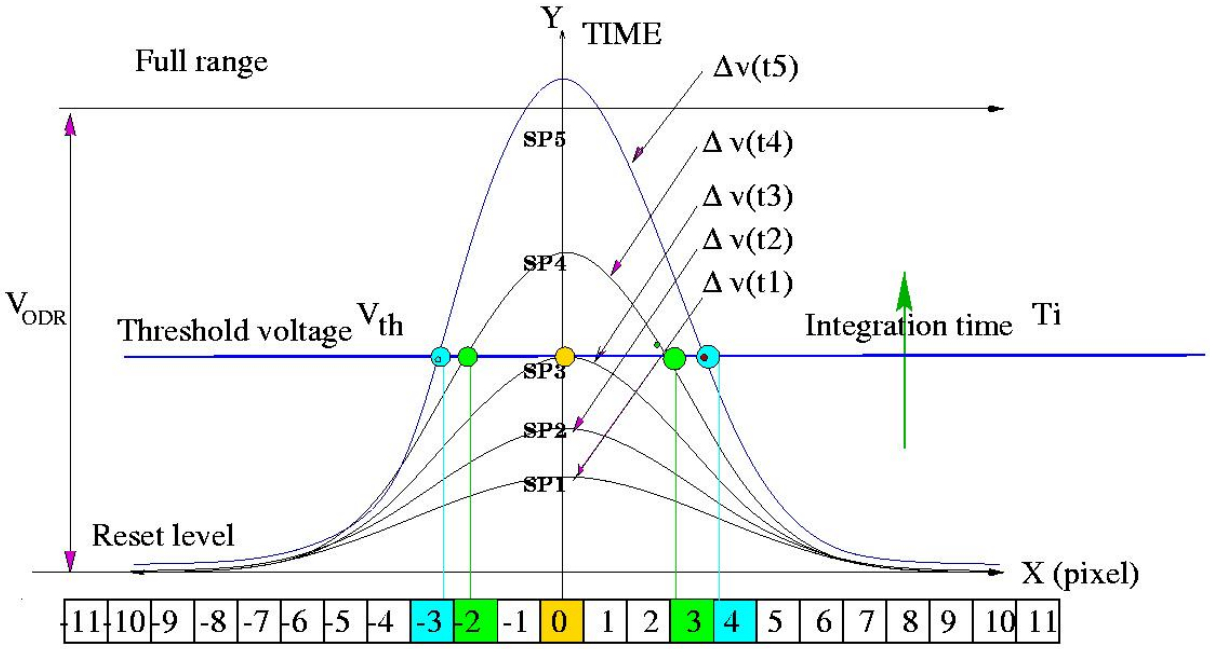

Figure 3.5: *Light spot position estimation through multiple thresholding technique.*

The optical signal generates a current proportional to the light impinging on the photodiode. This signal is detected by the photodiode working in storage-mode, and converted into a voltage drop, which for small voltage variations, is linearly related to the light intensity.

Therefore, the induced voltage drop can be expressed as:

$$\Delta v_k = \frac{\Re T_i}{C}\frac{D}{T}\int_{(k-\frac{1}{2})T}^{(k+\frac{1}{2})T} p(x)dx \qquad (3.11)$$

where, *R* is the photodiode responsivity measured in *A/W*, C is the photodiode capacitance, *Ti* the integration time, D is the photodiode length and T is the pixel pitch.

More in general, the voltage drop related to the k^{th} photodiode can be expressed as a function of the integration time (t):

$$\Delta v_k(t) = \frac{D}{T}\left(\frac{\Re}{C}\int_{(k-\frac{1}{2})T}^{(k+\frac{1}{2})T} p(x)dx\right)t\,; \quad \text{where} \quad t \le Ti \qquad (3.12)$$

The integral term on the right side of equation 3.12 can be simplified assuming that the light power density changes almost linearly along one single pixel.

Thus, the expression of *p(x)* can be replaced with the first order Taylor polynomial estimated at *k:*

$$p(x) \approx p_0\left[1-\frac{(kT-x_m)}{\sigma^2}(x-kT)\right]e^{-\frac{(kT-x_m)^2}{2\sigma^2}} \qquad (3.13)$$

and the k^{th} voltage variation will be:

$$v_k(t) \approx \frac{D}{T}\frac{\Re t}{C} p_0 \int_{(k-\frac{1}{2})T}^{(k+\frac{1}{2})T} \left[1 - \frac{(kT - x_m)}{\sigma^2}(x - kT)\right] e^{-\frac{(kT-x_m)^2}{2\sigma^2}} dx \tag{3.14}$$

Comparing the (M+1) voltages of the linear sensor with a threshold voltage V_T, two pixels can be detected corresponding to the two intersecting points, as shown in Figure 3.6.

$$V_T = \frac{\Re t p_0}{C} e^{-\frac{(x-x_m)^2}{2\sigma^2}} \tag{3.15}$$

Solving equation 3.15 with respect to *x*, the position of the two intersections can be calculated:

$$x_{1,2} = x_m \pm \sqrt{2}\sigma\left(\ln\frac{\Re p_0 t}{V_T C}\right)^{\frac{1}{2}} \tag{3.16}$$

and the positions of the related pixels of the sensor can be extracted by simply truncating $x_{1,2}$:

$$\begin{aligned} h_{VT} &= Int\frac{1}{T}\left(x_m + \sqrt{2}\sigma\left(\ln\frac{\Re p_0 t}{V_T C}\right)^{\frac{1}{2}}\right) \\ k_{VT} &= Int\frac{1}{T}\left(x_m - \sqrt{2}\sigma\left(\ln\frac{\Re p_0 t}{V_T C}\right)^{\frac{1}{2}}\right) \end{aligned} \tag{3.17}$$

for the coordinate (h, k). Int gives pixel value in integer. The mean value of the light spot is estimated with a resolution of ±(1/2)T:

$$x_{mVT} = \frac{(h_{VT} + k_{VT})T}{2} \tag{3.18}$$

If we execute this process for N different threshold values V_{Ti}, we obtain N pixel pairs and thus N new mean values, each one with a resolution of ±(1/2)T.

Combining all these values, we obtain a final spot position estimated with a much higher accuracy:

$$\bar{x} = \frac{1}{N}\sum_{i=1}^{N} x_{mi} \tag{3.19}$$

It has to be noted that, within the *N* pairs of pixels, there is a likelihood of repetition of a certain data occurrence. Due to this criteria, different threshold values have been chosen, as explained below. If we chose N thresholds uniformly distributed along the signal dynamic range, it could happen that, successive values of the threshold detect the same pixel pair. This case is more frequent if the threshold is close to the steepest zone of the Gaussian or in other words, where its second derivative is zero, which happens for:

$$x = \pm\sigma \tag{3.20}$$

Table 3.1: *Multiple occurrences of identical data*

Index i	Left		Right		Content of the Counter	Resolution ±	Sub-pixel resolution
	Pulse count	Pixel position	pixel position	Pulse count			
1	15	0	1	14	1	½	0.5
2	14	0	1	14	1	½	0.5
3	14	-1	1	14	1	0	0.33
4	14	-1	1	14	1	0	0.25
5	14	-1	1	14	1	0	0.20
6	14	-1	1	14	1	0	0.16
7	11	-4	4	11	1	0	0.14
8	11	-4	5	10	2	½	0.080
9	11	-4	5	10	3	½	0.065

The values in the Table 3.1 show instances of repetition of similar data sets. With 16th pixel as the origin, the left pixel at i=1 generates 15 pulses (giving the pixel at 0 as the first pixel crossing the threshold) and the right pixel generates 14 pulses (giving the pixel at 1 as the first pixel crossing the threshold from right). Hence, the content of the counter for i=1 is 1. By accumulating all the values, at i=9 the counter contains a pulse count of 3, which corresponds to having determined the location of the centroid with 0.065 of pixel precision (in terms of pixel value it will be 16 + 1 +0.065). If only 1 measurement was taken, this value would have been 0.5 pixel precision (in terms of pixel value it will be 16 + 1 +0.5).

It is also interesting to note that, at this point small translations of the spot position correspond to large variations of the signal values. This means the two pixels close to x = ± σ are the most sensitive with respect to the spot translations. Typically, in the *N* set of data this pixel pair has more occurrences than the others did.

Now, let us consider those pixels centred at σ and express the voltage variation related to a spot translation of Δxm:

$$\Delta v(\Delta x_m) = \frac{D}{T}\frac{\Re T_i}{C}\left(\int_{\sigma-\frac{T}{2}}^{\sigma+\frac{T}{2}} p(x)dx - \int_{\sigma+\Delta x_m-\frac{T}{2}}^{\sigma+\Delta x_m+\frac{T}{2}} p(x)dx\right) \tag{3.21}$$

By using the *p(x)* linearization of equation 3.13, the light spot position:

$$\Delta v(\Delta x_m) = \left(\frac{D}{T}\frac{\Re T_i}{C}\frac{p_0 e^{-\frac{1}{2}}T}{\sigma}\right)\Delta x_m \tag{3.22}$$

Equation 3.22 can also be expressed as:

$$\Delta v(\Delta x_m) = V_{ODR}\frac{\Delta x_m}{\sqrt{e}\sigma} \tag{3.23}$$

where V_{ODR} is the dynamic range of the voltage signal along the entire sensor:

$$V_{ODR} = \left(\frac{D}{T}\frac{\Re T_i}{C}p_0 T\right) \tag{3.24}$$

Equation 3.23 quantifies the sensitivity of a pixel placed at x = σ with respect to small translations of the Gaussian light spot. The shape of the spot is modelled by σ: the narrower the spot, the smaller the σ and the larger the Δv for a given spot translation Δx_m.

If we estimate the position using N different thresholds uniformly distributed along the sensor voltage dynamic range (V_{ODR}), the minimum pixel voltage variation to be detected has to be:

$$\min(\Delta v) = \frac{V_{ODR}}{N} \tag{3.25}$$

Using equation (3.25) in equation 3.23, we obtain that, for a given Gaussian light spot, there is a theoretical minimum number of thresholds to be used to achieve a position estimation sensitivity of Δx_m:

$$N \geq \frac{\sqrt{e}\sigma}{\Delta x_m} \tag{3.26}$$

In this case, the sensor sensitivity is defined as the minimum spatial shift (Δx_m) of the spot making the output signal a change of $(1/N)^{th}$ of the total signal range.

From equation 3.26, it can be observed that after a certain value of N, the sensitivity improvement is not more relevant when compared to the processing time and power consumption with the increased number of thresholding operations.

3.5.3 Algorithm implementation

The position estimation algorithm can be implemented both at pixel and array level. The main problem is related to the detection of the two pixels of the array, which are placed close to the intersecting points of the Gaussian equation and the current threshold.

Let us suppose to acquire an image and to binarize it with respect to a threshold voltage V_{th}.

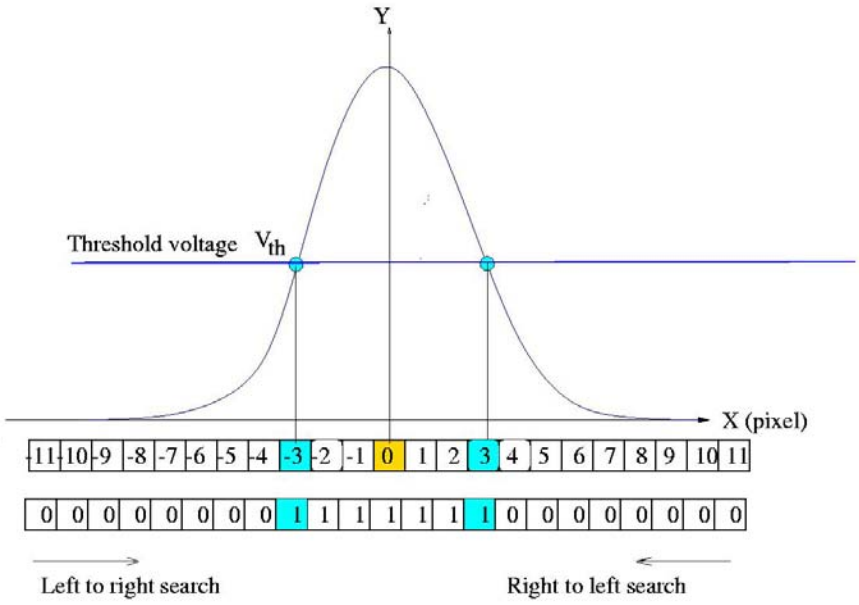

Figure 3.6: *Position to pulse conversion using a single threshold*

As shown in Figure 3.6, the two pixels (-3, +3) can be identified in two phases: from left to right, counting the number of pixels till the first 0→1 transition (e.g. 8 pixels); from right to left, counting the number of pixels till the first 0→1 transition (e.g. 8 pixels). By adding the first number (8) and subtracting the second one (8), will give the mean value of the spot within ±1/2 pixel pitch, which in this specific case is

0, corresponding to the pixel located in the middle of the linear array. Executing this operation with different threshold values will give different binary images and thus different mean values. By averaging all the N terms, the final position estimation value is given with higher accuracy.

All the above operations have to be executed at high speed and thus very close to the sensor. Hence, during algorithm implementation, some architectural constraints have to be taken in to account:

- The linear sensor has to be designed in order to be organized in a 2D array;
- Due to the large amount of data to be processed, the signal processing has to be fast in order to meet the sensor real-time requirements.

In order to satisfy the two main above mentioned requirements, it is decided to adopt a ***position-to-pulse conversion*** technique for detecting the two pixels related to one specific threshold value. This technique is very efficient for several reasons:

- The pixel searching procedure is sequential and makes the signal to be considered pixel by pixel along a single wire of connectivity, thus reducing the number of transistors per pixel;
- It is suitable to be implemented using asynchronous techniques reducing the problems related to the clock distribution which otherwise had to be addressed with a synchronous approach. The propagation time is also much faster and optimized with respect to the synchronous counterpart;
- This approach takes also into account the pixel modularity for design re-use;
- The generated pulses can be digitally processed with very simple operations and thus is extremely efficient in terms of silicon area.

3.5.3.1 Asynchronous position to pulse conversion

Asynchronous operation

The pulse-stream architecture employed here, being fully asynchronous, generates a digital burst with a frequency depending on the propagation delay between neighbouring pixels and thus only the pixels below the threshold voltage are involved in the search process.

To better describe the idea behind the position to pulse conversion, let us consider the example depicted in Figure 3.7. Two processing phases have to be considered: left to right (LTR) search process and right to left (RTL) search process.

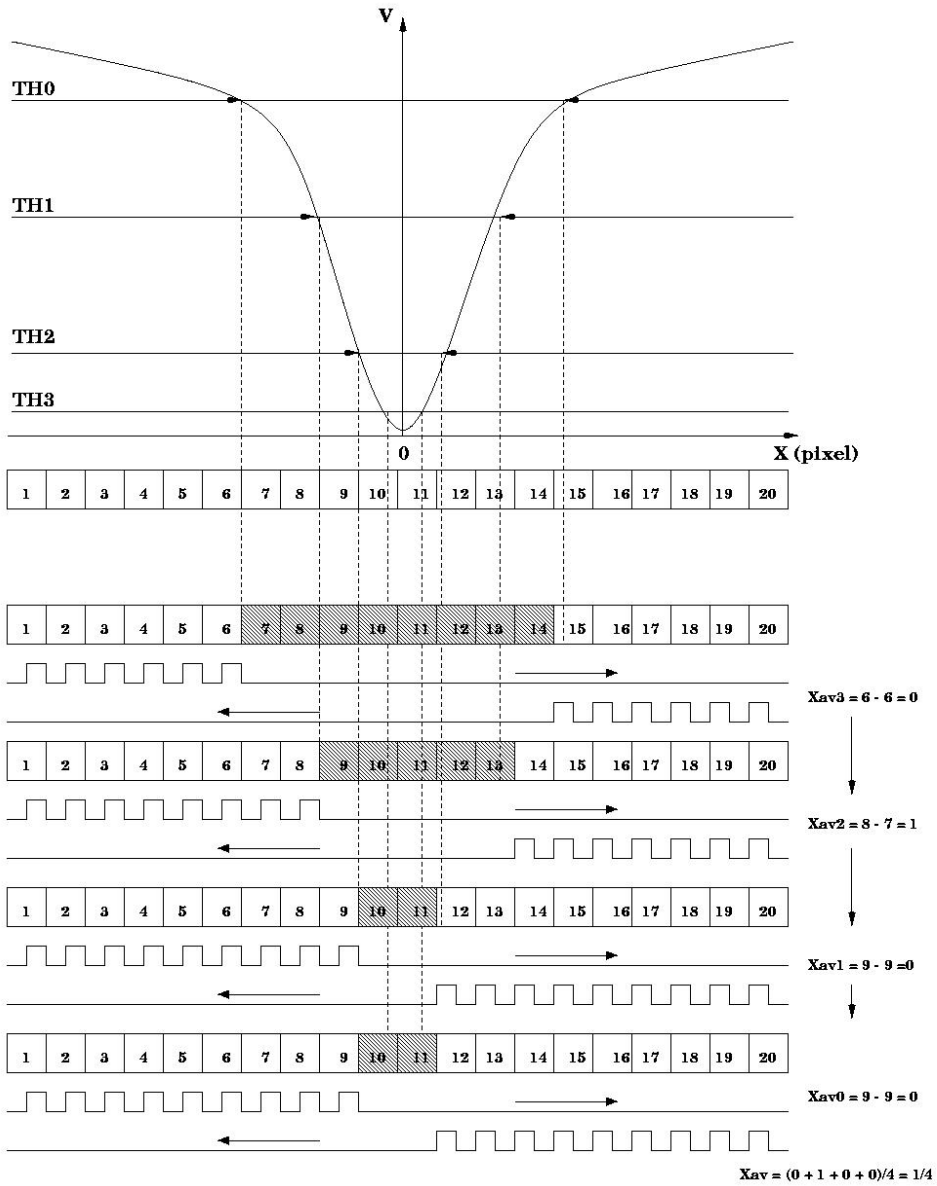

Figure 3.7: *Multiple thresholding method of extraction of centroid*

In the first phase, the signal of the leftmost pixel is compared with the threshold (e.g. TH0) and a single pulse will be generated onto a common bit-line only if the signal is larger than the threshold. After generating the pulse, the second pixel will be compared with the threshold and so on. The search process will continue until a pixel voltage is smaller than the threshold. Thus, the number of pulses generated along the bit-line corresponds to the number of pixels staying over the threshold, starting from left side of the linear sensor. The second phase, right to left search, follows the same principle starting from the rightmost pixel.

Referring to Figure 3.7 and considering the threshold TH0, in the LTR phase, 6 pulses are generated, the same as in the RTL process. By simply counting up the LTF pulses and counting down the RTL pulses, the mean value of the Gaussian is estimated related to a single threshold. Repeating this process with a different threshold voltage, and starting from the previous result, which in this specific case is zero, a new value is extracted corresponding to the estimated position over two thresholds. Considering threshold TH1, the final result is (6-6) + (8-7) = 1.

For example, by performing two measurements, the position estimate yields within ± ¼ T, four measurements yield ± 1/8 T and so on. While in theory one could achieve an arbitrary high precision, practical considerations limit the number of threshold voltages and the corresponding measurements.

3.5.4.1 Sub-pixel resolution

By binarizing the image continuously while integrating the light, the counter continuously outputs the difference between the up and down transitions. By observing the values one can obtain the deviation of the value from the ideal value. A typical operating cycle consists of an up and down computation followed by the delay (a loop). If we perform multiple operations during one integration cycle, the sub-pixel value can be calculated accurately as following:

By repeating the process for the N thresholds without clearing the counter, one accumulates the values of the midpoint locations, resulting in a determination of the centroid with a resolution of $\frac{1}{1+\log_2 N}$ T. For example, if one has an array of M = 32 pixels and performs N = 64 thresholding operations, one would need a counter of 5+7 =12 bits. If the loop (one up and down operating cycle value, which should be powers of 2) is 16, then the last 5 bits of the counter determine the sub-pixel value to the uncertainty of 1/16. Similarly, if the loop value is 128, the 8 bits of the counter value determine the sub-pixel resolution within 1/128.

A simple shifting of the resultant value does away with the need for any ALU to perform complex divisions or multiplications. For example, if a typical pixel value is represented in 12-bit binary as 0001.11010011, where the first 4 bits represent pixel number one, and the sub-pixel resolution by the following 8 bits.

Sample centroid calculation:

If the centroid is calculated with one set of readings, the accuracy can be expressed with

$\frac{Xup + Xdn}{2}$ which will be $\pm\frac{1}{2}$, meaning 1 bit resolution.

Ex: Considering an array of 31 pixels, if the up value is 15 and down value is 17, the counter counts up 15 and counts down up to 17 from 31 (31-17= 14). Hence, the effective counter contents is 15-14=1, in 12 bits, it is 0000 0000 0001. Considering 5 bits are for counting the pixels from -15 to +15, and the remaining 7 bits are for sub pixel resolution, the sub pixel value now is 000 0001, where the LSB indicates the $\pm\frac{1}{2}$ resolution. Now, if the centroid is to be calculated with multiple readings, for loop value 2^4, 5 bits are needed to calculate the sub pixel value, for loop value 2^5 , 6 bits and so on.

3.5.5 Overlapping the process operation with integration time

The multiple thresholding method requires specific threshold voltage generator. A different method of achieving sub-pixel resolution through multiple *images binarization* could be to use a single constant threshold voltage and running the image processing during with the integration time.

3.5.5.1 Multiple images binarization

By overlapping the integration time and processing time, the sensor's frame rate can be significantly improved, which is mainly limited by the number of processing cycles. During the integration time, the voltage profile of the light spot along the imager evolves, as shown in Figure 3.8. Right at the beginning of the integration time, Ti, the search process is started. For the example in the figure, this will result in the determination of the centre pixel (result = 0) because the counter counts up and down the same number of pulses for each processing cycle (this occurs for SP1 and SP2 in the figure).

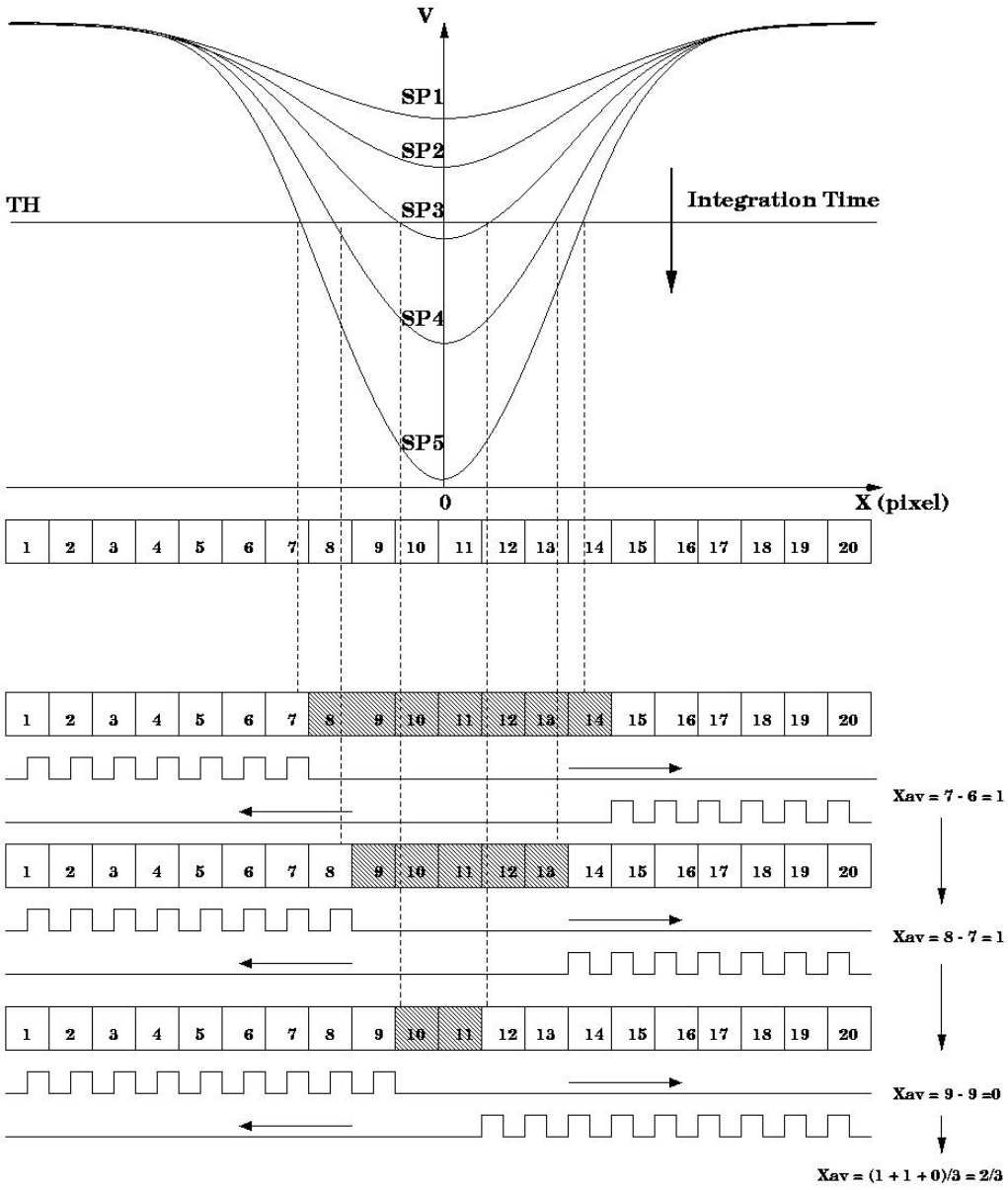

Figure 3.8: *Principle of operation with fixed threshold voltage*

Since the pixels continue to integrate the light after some time, some of them will reach a voltage that is below the threshold voltage (this occurs for SP3 in the figure), while the searching procedure continues as previously described.

The multiple images binarization can be thought of as an equivalent to the multiple thresholding. While in the former the multiple images are acquired based on different threshold voltages, in the latter multiple images are acquired in the time domain based on different integration times.

The main advantages foreseen here are the possibility to overlap the integration time and the processing time and the need of just one threshold to perform the multiple binarizations. This technique is experimentally investigated in this thesis and described in detail in the chapter on testing. The results are presented in Chapter 6.

All the linear arrays of the imager perform the processing of the signal in parallel, while the pixels of the same array proceed sequentially. The key idea is to use an enabling signal propagating along neighbouring pixels of each linear sensor. A pixel performs the comparison between its value and the threshold voltage only when this signal reaches it.

3.8 Up-down counting

This is divided into three parts: (i) Up/ forward counting (ii) down/reverse counting and (iii) up-down counting.

During the Up counting, the counter counts the number of pixels which have not crossed the threshold in the forward direction. The number varies from 1 to 31 (because the linear array is proposed to have 31 pixels) which means that if the count is 10, pixels up to and including 10^{th} pixel have not crossed the threshold and that pixel number 11 has crossed the threshold in the up/ forward direction. The counter increments the count to 10. Then the pixel crossing the threshold inhibits the *carryout* signal in propagating in the forward direction. The counter contains the binary equivalent of the count 10.

Similarly, during the down counting the counter counts the number of pixels, which have not crossed the threshold in the reverse direction. The number varies from 31 to 1 which means that if the pixel number 10 from right crosses the threshold, then the counter decrements its content by 10. The value available at the output of the counter is the pixel number with respect to the origin, which is generally the middle pixel of the array. In the case of 31 pixels, it is the pixel number 16. Once the pixel is activated it inhibits the previous pixel in accessing the bit line and prevents the *carryout* signal in propagating further. Figure 3.9 shows the Up/Down counting procedure.

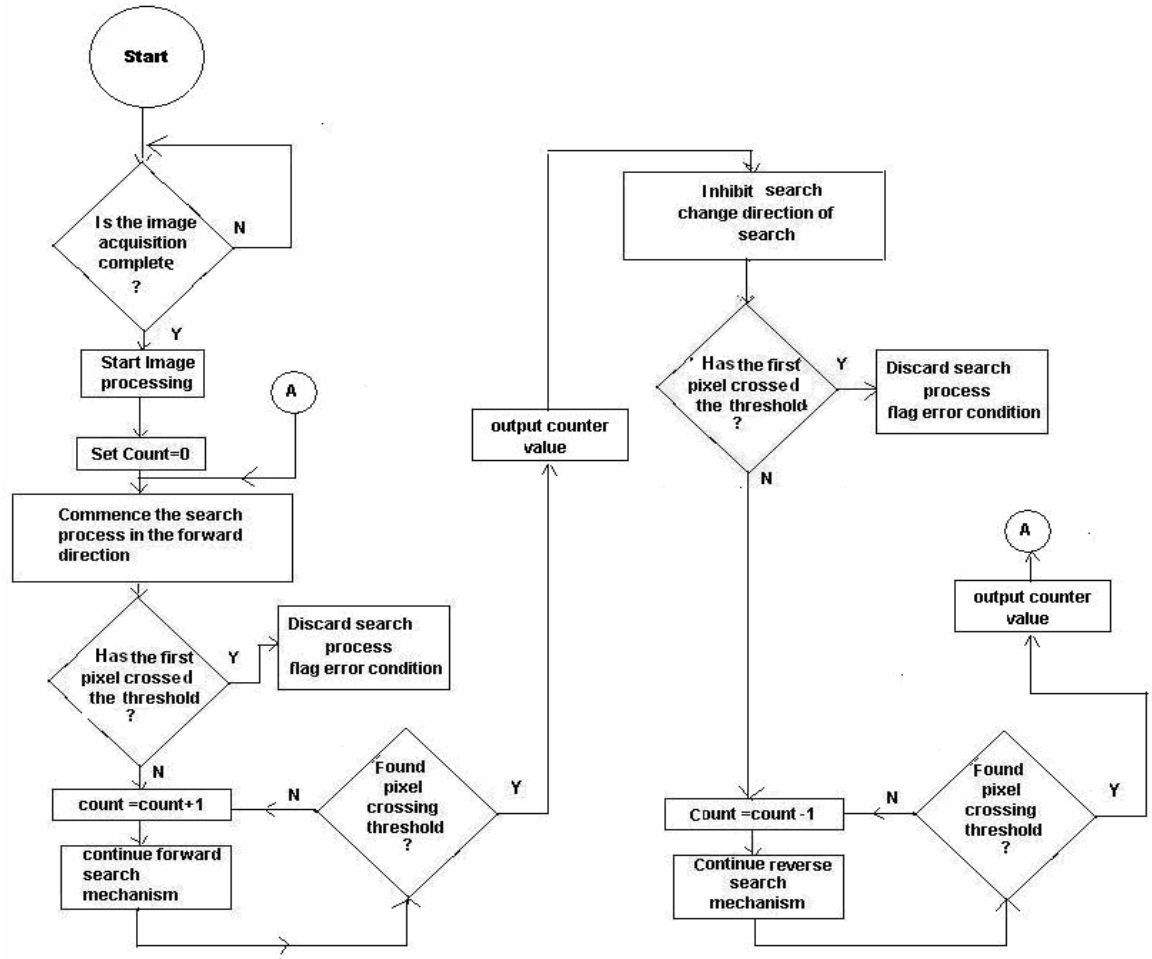

Figure 3.9: *Up/Down Counting mechanism in multiple thresholding method*

In practice, where the counting takes place in both the directions, the counter increments the count with the pixels not crossing the threshold in forward direction and decrements the count with the number of

pulses generated by the pixels in reverse direction. The counter effectively has the difference between the up and down counting. If the count in the Up direction is higher than that of the down direction, the counter will have a positive value identifying the index of a pixel right of the origin.

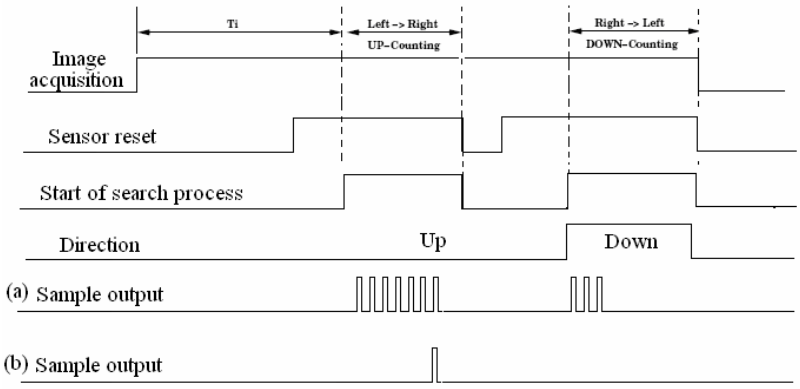

Figure 3.10: *Waveforms showing the concept of up/down counting corresponding to pixels 8 from left 3 from right (a) separate result (b) result of combined operation*

The waveforms show the result of a sample separate up & down counting. Sensor is taken out of reset state and the search process is initiated. Depending on the direction pulse, the outputs in forward and reverse directions can be observed, as shown in Figure 3.10. The provision to implement the up & down pulses separately, during the image acquisition, helps during debugging phase.

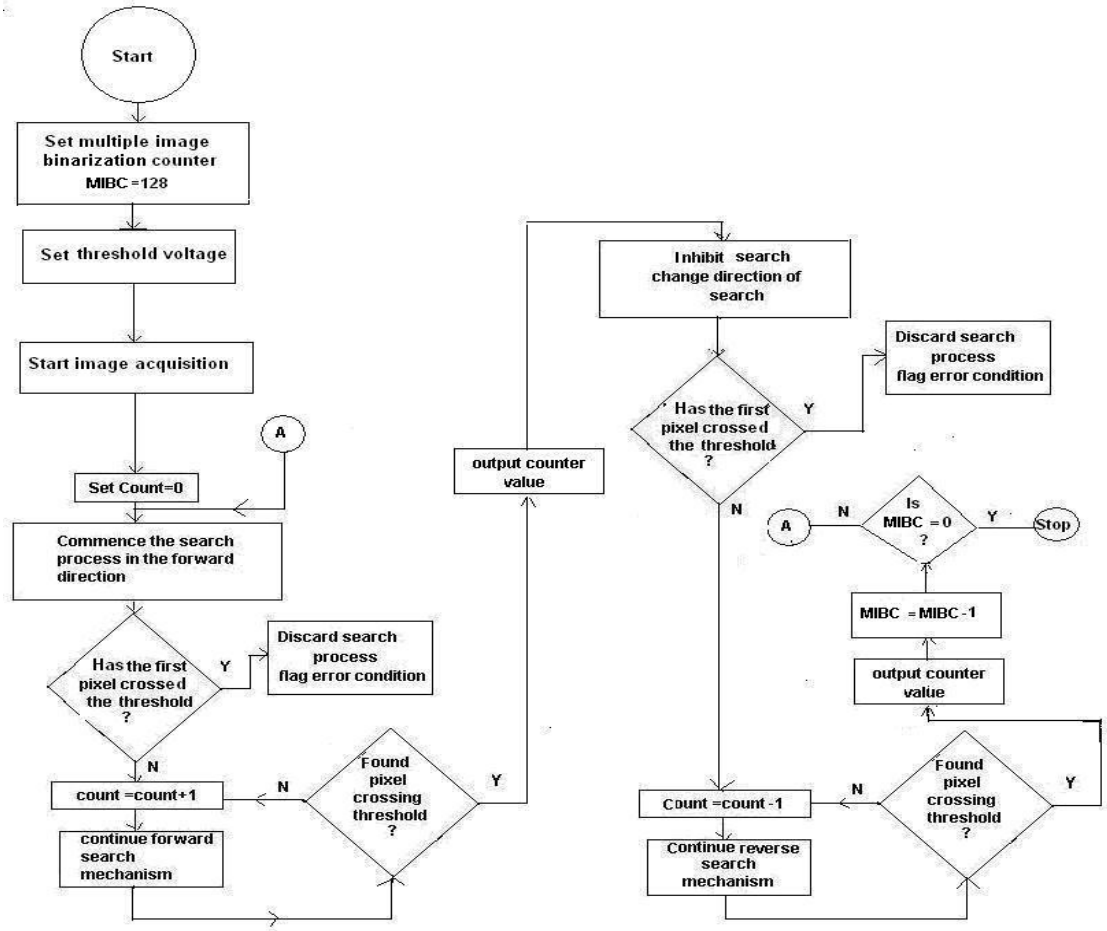

Figure 3.11: *Up/down counting in multiple images binarization*

If either pixel 1 or 31 are the ones crossing the threshold in both the directions, it is treated as error condition as the centroid cannot be determined with the value from only one direction.

For simplicity, it is preferred to have the origin at the middle of the array, i.e., pixel no. 16 and the light spot is focussed in such a way that the left transition is close to origin in the right and right transition to be as close to the left transition as possible, to have a sharp spot. This helps in calculating the spot in the positive axis.

Figure 3.11 shows the up/down counting with multiple images binarization method. Here, a counter MIBC is defined, which contains the number of operations intended to be undertaken, subject to the desirable sub-pixel value. Presetting the threshold voltage, the binarization operation is carried out on the similar lines of the multiple thresholding.

3.10 Parallel to Serial data conversion

The counter output consists of the pixel number and the corresponding sub-pixel resolution value. Interfacing a shift register with the counter will enable the data to be transmitted serially for post processing. This process can reduce a valuable chip area and pin number requirements. Interfacing serial data for post processing is also relatively less complex. However, it is to be noted that this is applicable only for a linear sensor and for the 2D sensor a different mechanism to be applied, which will be discussed in the next chapter.

3.11 Testing and testability

Incorporation of testability features saves painful debugging efforts and sometimes provides clues to otherwise seemingly a clueless and dead-end session. In this design, it is thought to provide full testability features. The linear array will be providing direct output (carryout) for checking the forward and reverse pixel to pixel propagation process when no pixel crosses the threshold. This helps in calibrating the sensor to accurately position itself to receive the light spot at the desired pixel value. Since, the carryout signal is activated if the pixels do not cross the threshold in either direction. The counting and serial data shifting stages are also to be considered for providing independent testability features since, during the debugging phase, the provision to count and output the values separately is a very useful feature.

3.12 Conclusion

This chapter has provided necessary background of phototransduction in CMOS photodiodes, and suggested the n^-/p^- as the choice of photodiode implementation due to its low junction capacitance. A detailed discussion on multiple thresholding algorithm is presented for estimating centroid position with sub-pixel resolution. Using a fixed threshold and binarizing multiple images in one frame explored the feasibility of sub-pixel resolution, treating time as an equivalent parameter of voltage of the multiple thresholding algorithm. The implementation of this algorithm in CMOS VLSI is discussed in the next chapter. Also presented is a discussion on the asynchronous position to pulse conversion technique for efficient conversion of the analog photo signal in to digital domain, the mechanism of up/down counting and the need for incorporating testability features in the device.

Chapter 4

Sensor Design

4. 1 Introduction

This chapter describes the design of the smart linear sensor performing single light spot digital position estimation. This sensor will be the basic functional block of a 2D image sensor architecture for range finding.

4.1.1 The 2D Sensor

The sensor design is proposed to be a closely packed array of N identical linear sensors, working in parallel, as shown in Figure 4.1. Each linear sensor consists of two sub blocks: an (M+1) pixel linear array, and a digital processor block implementing the position estimation algorithm.

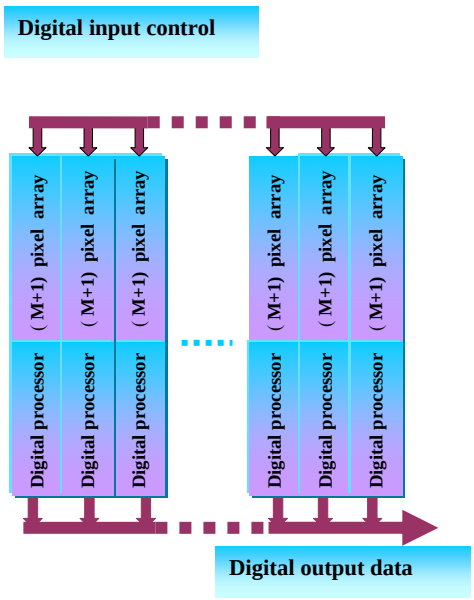

Figure 4.1: *2D smart image sensor block diagram*

Common inputs drive the linear sensors and the output of each linear sensor is available on the digital bus. The scheme mentioned in this section is a generic one. As the design evolves through the end of this chapter, an extension to the two-dimensional architecture presented, considers all the design issues.

The majority of this chapter is devoted to the design of the single linear smart sensor consisting of two main parts, the linear array and the digital processor.

4.2 The linear sensor array

As shown in Figure 4.2, each linear sensor array consists of (M+1) pixels performing image acquisition, image binarization and position-to-pulse conversion. The digital processor collects the pulse bursts coming from the linear sensor and filters them in order to extract the final position estimation.

For each new frame, a number of images are binarized with different threshold values, depending on the desired sub-pixel resolution (more on this in the chapter on results). For each binary image, the position-to-pulse conversion process is run in order to detect the position of the two most external pixels related to the transition. The search process is divided in two phases: search of the first transition from top side of the sensor to the bottom (**forward** or **up**); search of the first transition from bottom side of the sensor up to the top (**backward** or **down**).

With the digital control block initiating the search process, the first pixel in the array receiving the 'START' signal commences the search for the pixel crossing the threshold in the forward direction.

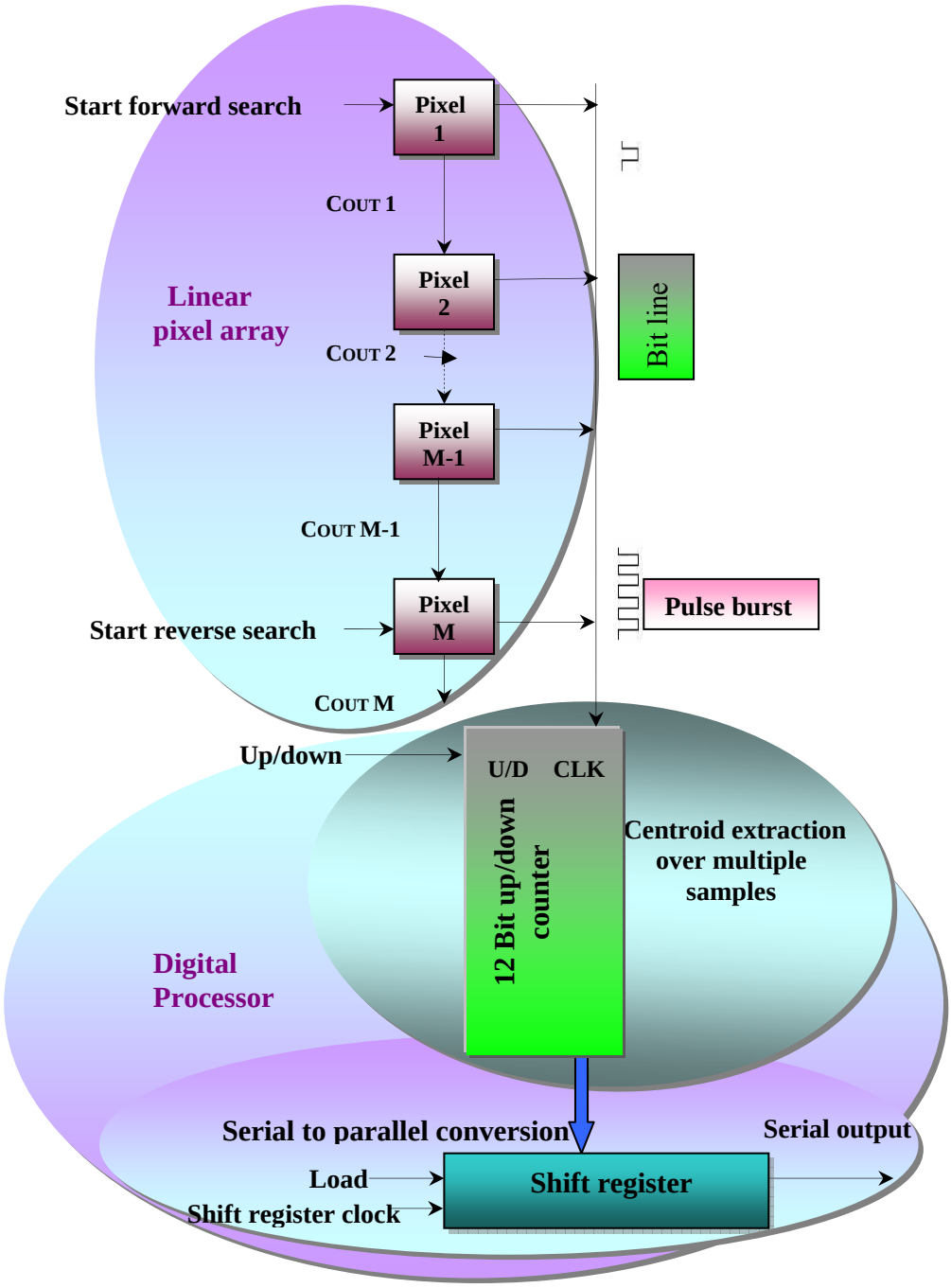

Figure 4.2: *Block diagram of the pixel array*

This process does not need a global clock since the participating pixels themselves generate the enabling signal. The first pixel initiates the search process and generates a self-driven clock or enabling signal; a carry (COUT1) for propagating along the array (COUTi for the i^{th} pixel). This signal generation is dependent on the propagation delay of each pixel. With this enabling signal, the first pixel interrogates the second pixel; the second interrogates the third and so on, until the end of the array or until a pixel crossing the threshold, whichever occurs first.

As long as a pixel does not cross the threshold, it generates a pulse and adds to the pulse burst on the bit-line; and the counter increment its value. Hence, at any instance the counter contains the index of the latest pixel that is unable to cross the threshold. When a pixel crosses the threshold, the computation ceases in the forward direction and starts in the reverse direction. The process in the reverse direction is identi-

cal, but the counter value is decremented. Thus, at any instance the counter shows the updated value considering the computation both in the forward and reverse directions. At the end of one operating cycle, the counter contains the estimation of the position of the centroid of the Gaussian distribution: corresponding to the threshold value under consideration, the linear array receives in one frame.

4.2.1 Carryout signal propagation time

The worst-case occurs when the light, impinging onto the sensor, is not enough to make any pixels cross the threshold. This could happen when the light spot is outside the sensor array. In this case, the search process generates a burst of (M+1) pulses, equivalent to the number of pixels in the array, on the bit-line and propagates the carry to the end of the array.

The burst on the bit-line is generated with a pulse repetition depending on the intrinsic pixel propagation delay, since the implemented search process is asynchronous. Therefore, the maximum time required to execute the search operation in one direction, is given by:

$$T_{exm} = (M+1)\,\tau \qquad (4.1)$$

where τ is the pixel propagation delay and M is the number of pixels of the linear array.

The computation does not start in reverse direction immediately after a pixel crossing the threshold in forward direction, since there is no mechanism in the circuit to reverse the search direction until the T_{exm} is completed. Hence, the time taken for the search process in each direction always remains the same and depends on the pixel count.

4.2.1 Pixel Architecture

Figure 4.3 shows the block diagram of the pixel. It consists of a reset transistor, a photodiode, a comparator, a pulse generation block and a carryout generation block. The photodiode is reset to V_{res} by the transistor MRES and released with PHRES signal. The output of the photodiode, V_{pix} connects to the differential clocked comparator along with a threshold voltage input V_{th}, and a clock input from the previous pixel in the array. If it is the first pixel, the comparator gets START pulse from the digital input control lines. The difference between V_{pix} and V_{th} determines whether to propagate the carry forward to continue the search process and generate a pulse (to identify the pixel position) or to output a signal indicating that

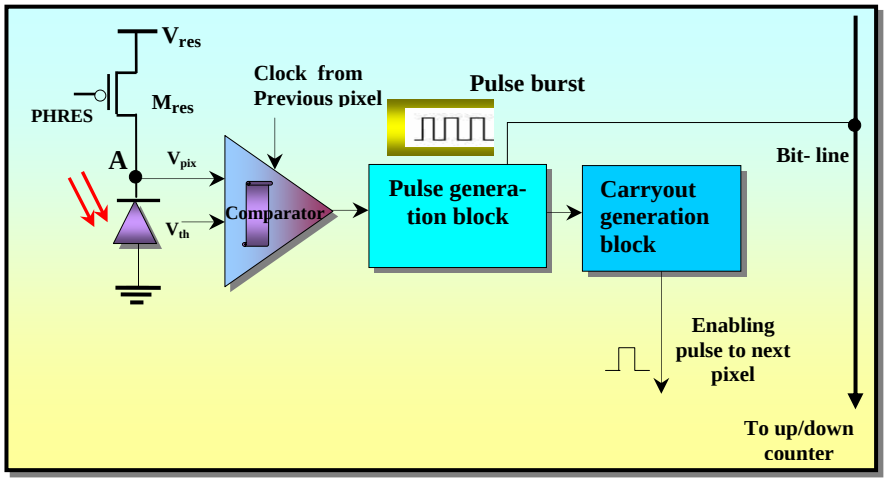

Figure 4.3: *Pixel functional block diagram*

no pixel has crossed the threshold. Table 4.1 indicates the status of the operation. As the design considers pixel level processing, it is appropriate that the pixel itself does the digitization of the photo input signal. A high speed 1 bit ADC is implemented at pixel level. Binarization close to the photo generated signal means also simple circuitry (few transistors) and relaxed architecture speed specifications. The following subsections describe individual blocks of the pixel.

Table 4.1*: Status indication after one cycle of operation*

V_{res} & V_{th} relation	Pixel(s) status	Bit-line status	Carry-out pulse
$V_{res}<V_{th}$ Case (i)	If the first pixel crosses the threshold	No pulses on the bit-line	0
$V_{res}<V_{th}$ Case (ii)	If k^{th} pixel crosses the threshold	k-1 pulses in the pulse burst on the bit - line	0
$V_{res}>V_{th}$	None of the (M+1) pixels in the array crosses the threshold	M pulses on the bit-line	1

4.2.1.1 Sensing node capacitance

The photodiode works in storage mode (as explained in the previous chapter) conditions and is periodically reset to V_{res} by means of the transistor M_{res}. During the integration time (T_i), the photodiode integrates the light received from a synchronized light source and provides output voltage drop, which is, in first approximation, linearly proportional to the light intensity, for small voltage variations.

The photodiode needs to have high sensitivity in order to generate maximum voltage proportional to the incident light. In the real case, parasitic capacitances, connected to the photodiode, reduce the conversion factor, because they only increase the total node capacitance without contributing to the signal collection. The sensing node (A) capacitance can be expressed with:

$$C_{pix} = C_{cd} + C_{dMres} + C_{gdOV} + C_{comp} \tag{4.2}$$

where C_{cd} is the diode diffusion capacitance, Cd_{Mres} and C_{gdOV} are the drain capacitance and the gate-drain overlapping capacitance of the reset transistor Mres respectively, and C_{comp} is the input capacitance of the comparator.

The diode junction capacitance is given by

$$C_{Cd} = \frac{A.Cj_{NW}}{\left(1+\frac{V_d}{PB}\right)^{MjNW}} + \frac{P.C_{jsNW}}{\left(1+\frac{V_d}{PB}\right)^{MjsNW}} \tag{4.3}$$

Where A and P are the diode area and perimeter, C_{jNW} and C_{jsNW} are the area and side wall junction capacitance respectively. MjNW and MjsNW are area and sidewall grading coefficients and PB is the junction potential. Considering a reverse bias voltage of V_d = 2.0 V and using technology parameters (AMS CMOS .35um CXQ process parameters, confidential), Equation 4.3 gives a value of about 50.575 fF. In the design, the area of the integrating photodiode is 486 μm^2.

The drain diffusion capacitance is calculated as follows:

$$C_{dMres} = \frac{A.Cj_{dd}}{\left(1+\frac{Vd}{PB}\right)^{Mjdd}} + \frac{P.C_{jsdd}}{\left(1+\frac{Vd}{PB}\right)^{Mjsdd}} \tag{4.4}$$

C_{dMres} calculated from the process parameters is 4.574 fF.

The gate - drain overlapping capacitance of PMOS (reset transistor) is calculated as follows:

$$C_{ov} = C_{gdov}[F/um]W \tag{4.5}$$

And is given by AMS process as 0.086fF/μm.

The comparator input capacitance is calculated as:

$$C_{comp} = C_{ox}WL + 2CovW + 2LC_{gbo} \quad (4.6)$$

Where C_{gbo} is the bulk overlap capacitance of the input transistor.

Cov = 0.12 fF/ μm for NMOS, C_{ox} is 4.54 fF/μm^2, W = 1μm, L=0.3μm, C_{gbo}=0.11 fF/μm

⇨ C_{comp} = 1.668 fF

Therefore, the total capacitance at the node is given by the sum of equations 4.3, 4.4, 4.5 and 4.6 and is calculated as 55.149 fF.

Here, the capacitance that is contributing to integrating the light is the photodiode capacitance C_{cd}. The capacitances, C_{Mres} and C_{comp} do not contribute to light detection. Hence, both terms should be low, to have minimum effect on the node capacitance. Though M1 contributes to node capacitance and M2 does not, the size of M1 is dependent on M2, as M1 & M2 (explained in next section) are the differential pair of the comparator and should be identical. To avoid mismatch, they should be large. However, larger size transistor increases the node capacitance. Hence, these transistors sizes are to be chosen considering their contribution to be minimum to the node capacitance but having large enough area to avoid mismatch. By default, all the transistor sizes are taken to be minimum except for those in the slow inverters in pixel and the feedback circuits.

The voltage drop at the sensing node is given by

$$\Delta V = \frac{I_{ph}.\Delta T}{C_{pix}} \quad (4.7)$$

where I_{ph} is the photodiode current, ΔT is the integration time, C_{pix} is the total node capacitance.
I_{ph} can be expressed as:

$$I_{ph} = \Re.P_d.A_d \quad (4.8)$$

where R is the photodiode spectral responsivity measured in A/W defined by the ratio (expressed in A/W) of the photo generated current I_{ph} over the optical power incident on the sensor, P_d (W/μm^2) and A_d (μm^2) is the active area of the photodiode.

$$\Re = \frac{I_{ph}}{P_d} \quad (4.9)$$

Replacing these terms in equation (4.7):

$$\Delta V_{pix} = \frac{\Re.P_d.A_d.\Delta Ti}{C_{pix}} \quad (4.10)$$

In the expression 4.10 the term A_d, is only due to the photodiode, while C_{pix} is due to all the capacitors connected to the sensing node. Therefore, for a given photodiode geometry, the highest conversion factor can be reached by minimizing the value of C_{pix}. Equation 4.10 gives the change in voltage at V_{pix} during the integration time ΔTi.

Since the optical power is a function of the number of photons forming the optical beam, n_{ph} and of the energy of such photons:

$$P_d = n_{ph}.E_{ph} \quad (4.11)$$

The photo generated current is directly proportional to the number of electron-hole pairs generated and collected, n_e,

$$I_{ph} = n_e.q \quad (4.12)$$

The spectral responsivity can be expressed as a function of the quantum efficiency, η, as [SZE]:

$$R = \frac{n_e.q}{h.\frac{c}{\lambda}.n_{ph}} = \frac{n_e}{n_{ph}}\frac{q.\lambda}{h.c} = \eta.\frac{\lambda(\mu m)}{1.24} \tag{4.13}$$

The dark current can be estimated by means of

$$I_{dk} = JS_{NW}.A_{diode} + JSSW_{NW}.Pdiode \tag{4.14}$$

Where JSNW (0.06 fA/μm^2) and JSSWNW (0.27 fA/μm) are the area and sidewall leakage current values respectively. For an n-well/Psub diode reverse biased at 3.3 volts, the equation 4.14 gives a leakage current value I_{dk}=52.92 fA. Approximating the I_{dk} (V_r) with a square root function of the reverse bias voltage V_r, we can estimate the value of the leakage current at 2.0 V reverse bias voltage:

$$I_{dk}(2.0V) = 52.92\,fA \times \frac{\sqrt{2.0}}{\sqrt{3.3}} \approx 41.3 \text{ fA} \tag{4.15}$$

Since the photodiode has high output impedance, a source follower is usually introduced after the photodiode stage to reduce the impedance. However, each source follower has a gain < 1 and adds a dc bias current around a few hundred nA. For an array of 100 x100 pixels, the dc current of the sensor could reach the mA range. Hence, it is not convenient in this case to introduce a source follower.

4.2.1.2 Comparator block

The design of the high-speed, positive feedback, dynamic, clocked comparator [WAN] used in the pixel, as shown in Figure 4.5, directly affects the speed and power dissipation of the overall imager.

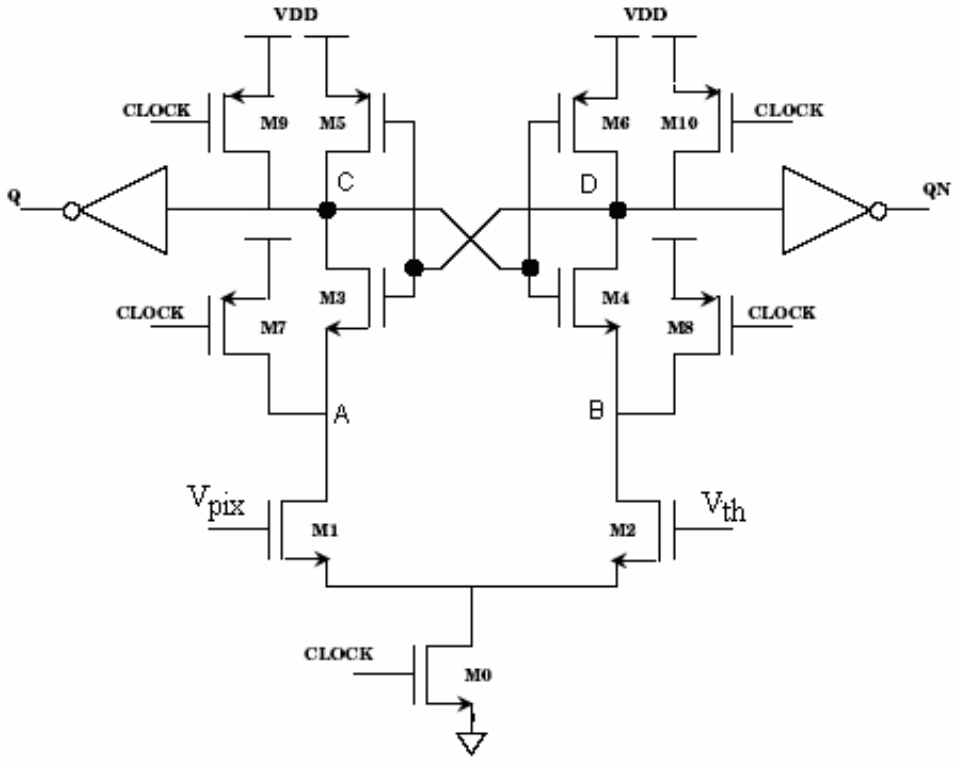

Figure 4.5: *Schematic of the fully differential clocked comparator*

The comparator compares the signal (V_{pix}) with the selected voltage threshold (V_{th}). When CLOCK is low, M0 is off, M5–M10 are on, and nodes A,B,C and D are pre-charged to VDD, placing the comparator

in the reset mode. When CLOCK goes high, M0 turns ON and M1-M2 compare the input threshold voltage V_{th} with the pixel voltage V_{pix}. Since M5– M10 are initially off, the resulting differential current first flows through the total capacitance seen at nodes A and B, creating a differential voltage at these nodes by the time M3 and M4 turn on. After the cross-coupled devices turn on, the circuit re-generatively amplifies the voltage, producing rail-to-rail swings at C and D.

The two main advantages of this comparator are: zero static power dissipation; and single-phase clock, which greatly simplifies the routing across the chip.

4.2.1.3 *Carryout* generation block

If no pixels are found crossing the threshold voltage during the search operation, the carryout generation block generates the *carryout* signal in forward and reverse directions for each search operation. This signal is particularly useful while testing the sensor with the coherent light spot.

4.2.1.4 Pulse generation block

Each pixel that does not cross the threshold voltage outputs a pulse on the bit-line. Thus, by counting the pulses on the bit-line, the index of the last pixel that did not cross the threshold can be found. At this point, the process stops the *carryout* propagation to the successive pixels. This is performed both in forward and reverse directions.

4.2.1.5 Functionality of the pixel

Figure 4.7 shows the schematic of the pixel. Q_j is the comparator output and C_{koj} is the enabling signal generated by the pixel. Q_{j+1} and Q_{j-1} are the outputs of the comparators in the forward and reverse direction respectively. C_{koj+1} and C_{koj-1} are the enabling signals from pixels in the forward and reverse directions (It may be noted that the transistors M1 to M6 are different from those used in the comparator).

Initially the photodiode is pre-charged at the reset voltage. During the integration time, the photodiode, connected to the inverting input of the comparator, is released from the reset and begins to discharge depending on the light intensity. Its voltage is compared periodically with the threshold voltage V_{th}, by clocking the comparator.

The bit-lines BLF and BLB are used to auto adapt the pulses generated during the search process in forward and reverse directions. The pixel generates a pulse by discharging BLF through M1 and M2. The signal propagates to the end of the array until the counter and returns with a certain delay through BLB. The BLB enables the pixel to charge up BLF in order to complete the pulse and propagate the enable signal to the next pixel in order to continue the searching process.

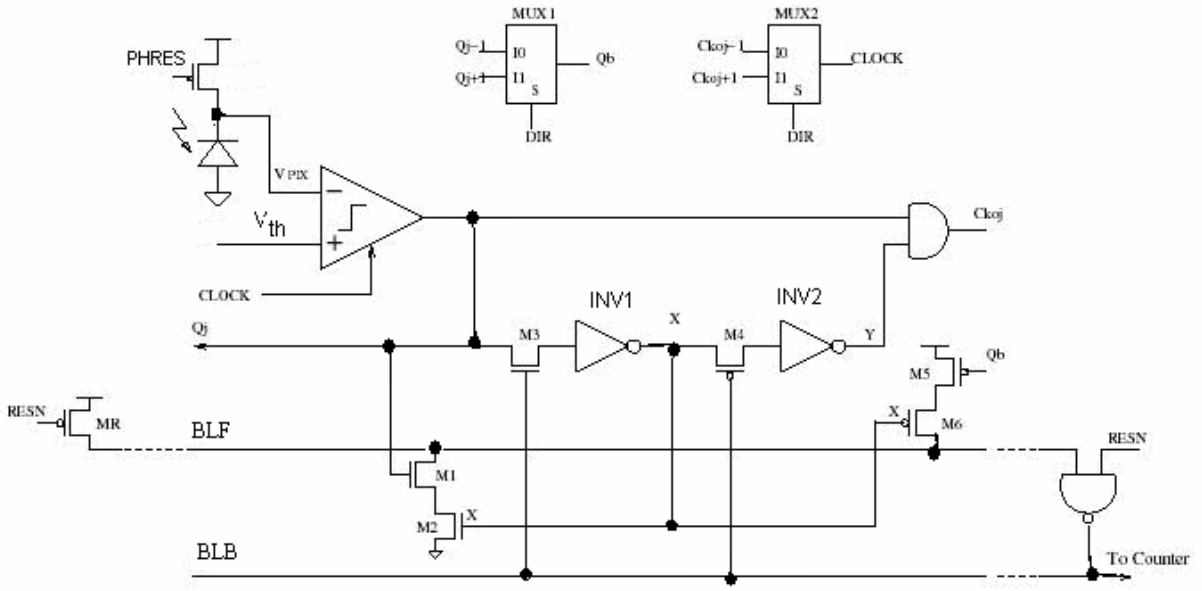

Figure 4.7: *Schematic of the pixel*

The two – input multiplexers MUX1 & MUX2 in the pixel generate Qb and CLOCK signal in the forward and reverse directions, to feed the Qj input of previous stage in the array, in conjunction with Qj1 (comparator output) and DIR signal.

When the CLOCK is high, the comparator output (Qj) may switch to high level depending on the value of the first pixel input(if $V_{pix}<V_{th}$) and disables the previous cell (from the second pixel onwards). This also enables the generation of *carryout* by feeding one input of the AND gate, which requires a second input.

4.2.1.6 Initialization procedure

Before starting the search operation, an initialization procedure has to be executed. The input signal START, connected to the comparator CLOCK of the first pixel of the imager, is set to 0, blocking the comparator's clock propagation. The second signal Y, responsible for clock propagation, has to be pre-set to 0 before starting the search process. This can be accomplished by pre-charging BLF through MR (RESN=O) and releasing it again.

With RESN=O, the bit-line BLB=1 forcing X notQj = 1; with RESN=1, BLB=0 and Y=notX=0. At this point the imager is ready for the image processing. During the integration time, the comparator of each pixel is under reset. The sensor's integration time (Ti) is defined by the time between the rising edges of PHRES and START respectively.

4.2.1.8 Search process

At the rising edge of START, if Vth > V_{pix}, then the output of the comparator is set to Q = 1, discharging the bit-line BLF through M1 and M2. After Δt_1, due to the propagation delay of the RC network consisting of BLF and BLB, transistor M3 is set making the node X to switch to 0. This makes BLF to be precharged through M5, M6, restoring the bit-line initial conditions. After the same Δt_1, BLB turns off, setting Y to1, which forces C_{KOJ} =1. This completes one operating cycle generating a single digital pulse onto the bit-line before propagating the comparator's clock to the next pixel. As already noted, the above operations are executed only if the current pixel satisfies the conditions: $V_{th} > V_{pix}$. If Vth < V_{pix}, the comparator does not switch, thus stopping the search algorithm. In this case, no pulse is generated onto the bit-line and no propagation clock is enabled.

4.2.1.9 Search process in the reverse direction

After the left to right searching process is completed, the same operation is executed backward by simply inverting the pixel connectivity without resetting the photodiodes. This is accomplished by setting the MUX1 and MUX2.

IN this prototype, the Inverters are custom built and made slow in order to avoid a potential conflict between the pulse generation on bit-line and the carry out propagation among the pixels.

4.2.1.10 Layout of the pixel

The layout criterion adapted here enforces strict measure on width of the array as the 2D sensor is considered a closely packed array of linear sensors. Hence, the width of the digital processor also should be considered within the same limit. Moreover, to provide a high fill factor, the photodiode is designed with a large area. The pixel accommodating 40 transistors cannot take any arbitrary pitch, the pitch of the pixel and that of the array are taken as the limiting factors. The associated circuitry also has been matched with the same dimension of the pixel. Figure 4.8 shows the layout of the pixel with 45 μm x 40 μm dimension and consists of 40 transistors. The fill factor is ~27%.

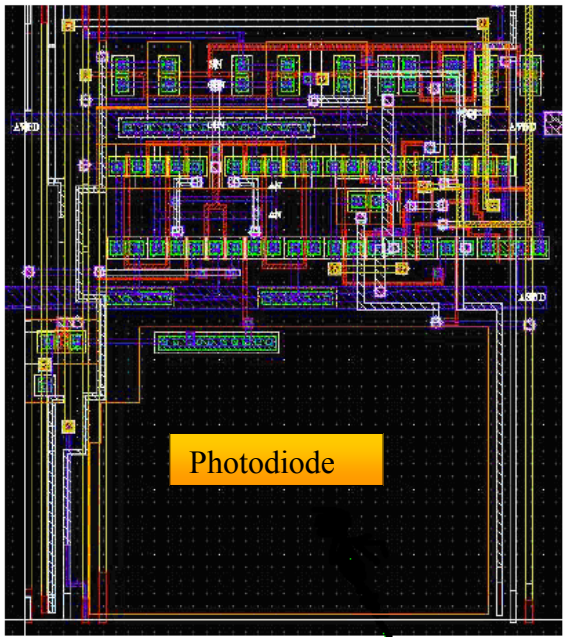

Figure 4.8: *Layout of the pixel*

4.2.1.12 Pixel Array

Figure 4.9 shows the block diagram of the linear array. For convenience, pixels 1, 2, 30 and 31 are shown. Photodiode signal in each pixel is terminated as V_{pix}. CIN is the 'START' signal as described in the initialization procedure. *Carryout* (COUT) signal is generated by multiplexing the CO0 and DIR in the forward direction and CARRY and DIR in the reverse direction. When the DIR is low (the forward search), the array output CO0 is the *carryout* signal in forward direction. When the DIR is high (reverse search), the array outputs CARRY is the *carryout* signal in reverse direction.

Similarly the MUX1 & MUX2 in the pixel generate Q_{j+1} and Q_{j-1} signals in the forward and reverse directions, to feed the Q_j input of previous stage in the array, in conjunction with Q_{j1}(comparator output) & DIR signal.

Ci1 & Ci0 in conjunction with DIR signal generates CLOCK in forward and reverse directions to feed the CLOCK inputs of the comparators from the second stage onwards.

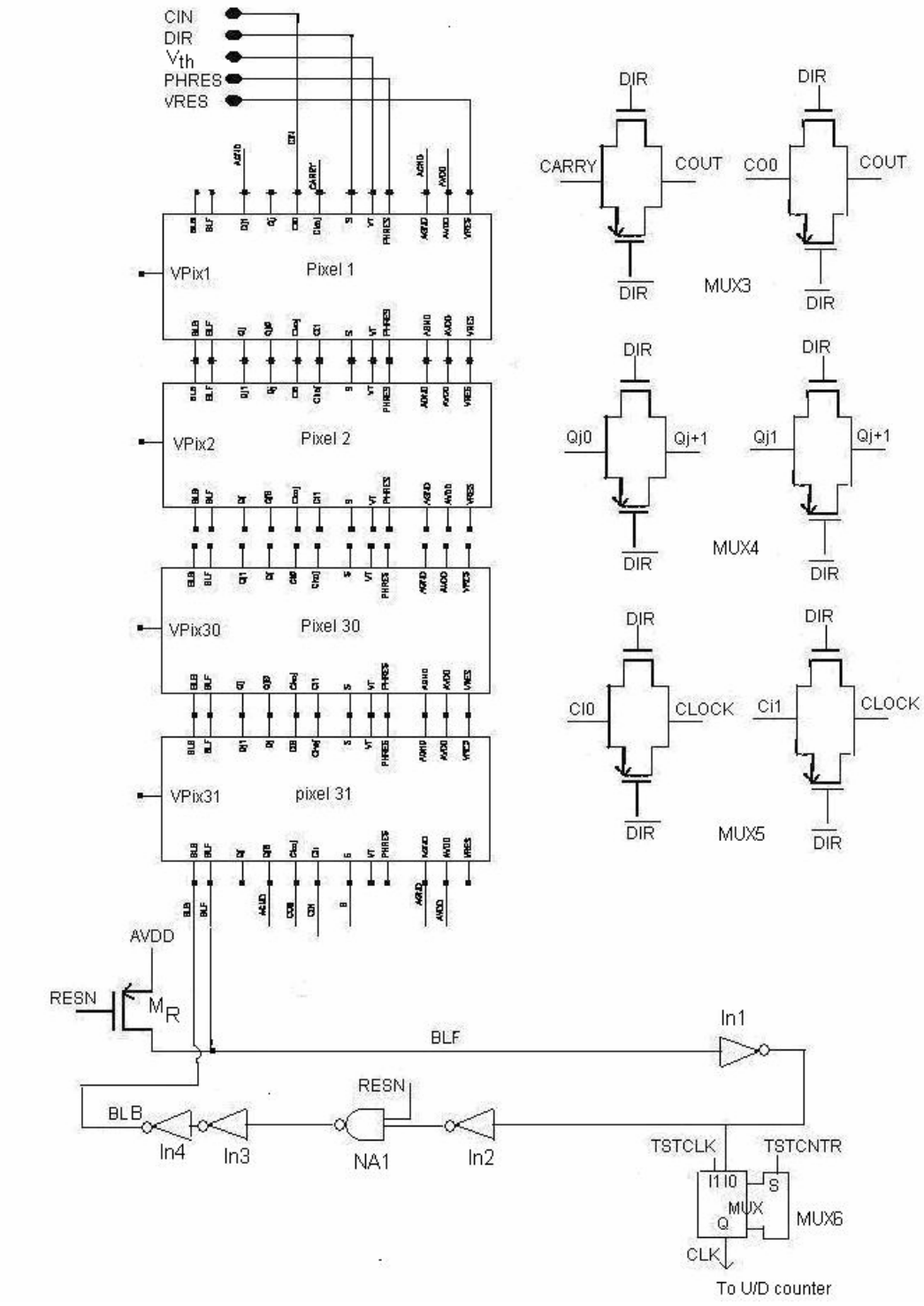

Figure 4.9: *Interconnections of the pixels and generation of control signals with multiplexers*

A timing diagram of the linear sensor, as shown in Figure 4.10, illustrates the operational sequence of the pixel array. After the integration time Ti, the light source is turned off and the search algorithm is started from left to right on the rising edge of START. The counter accumulates the number of pulses generated on to the bit line BLB. After completion of this phase, START is pulled down and the direction of the search process is inverted with DIR =1 and a new rising edge of START is applied. During the second phase, the counter works in down-counting mode subtracting the number of pulses from the previous

value. The output pulses in the forward direction indicate that pixel 8 from the left and pixel 4 from the right have crossed the threshold.

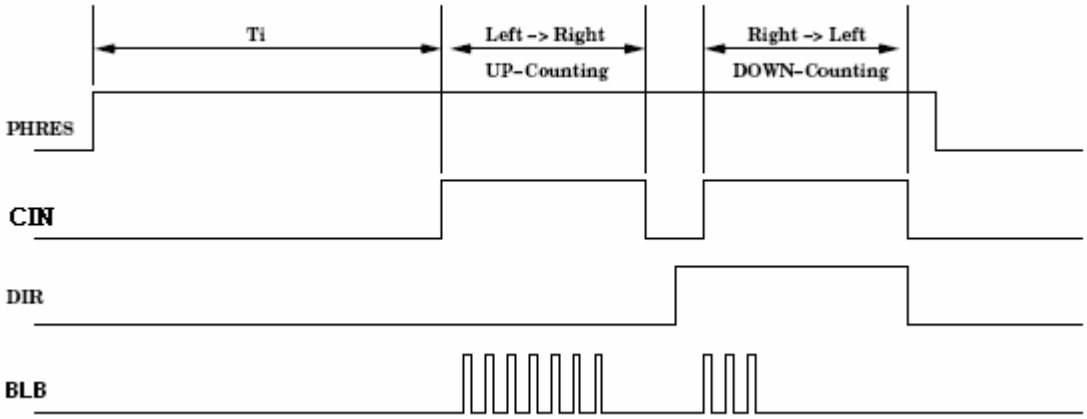

Figure 4.10: *One operating cycle in which pulse bursts are generated in the forward and reverse directions*

4.3. Digital processor

This section consists of (i) the centroid estimation performed by the combination of CLK signal of linear array and the up/down counter and (ii) the parallel to serial conversion performed by the shift register.

4.3.1 Up / Down counter

A ripple-chain up/down 12 bit binary counter [STA] is adapted to increment the counter value during the first processing phase (i.e. forward direction) and decrement the same during the second phase (i.e. reverse direction) and hence, the counter contains the effective pixel value after every operating cycle. Since the 12 bit counter can provide at most 7 bits for the sub pixel value (5 bits for counting the 31 pixels), only a maximum of (loop= 2^6) 64 thresholds can be performed. The counter needs to be larger if more thresholds are to be accounted for higher sub pixel resolution. More on this will be discussed in the Chapter on measurements.

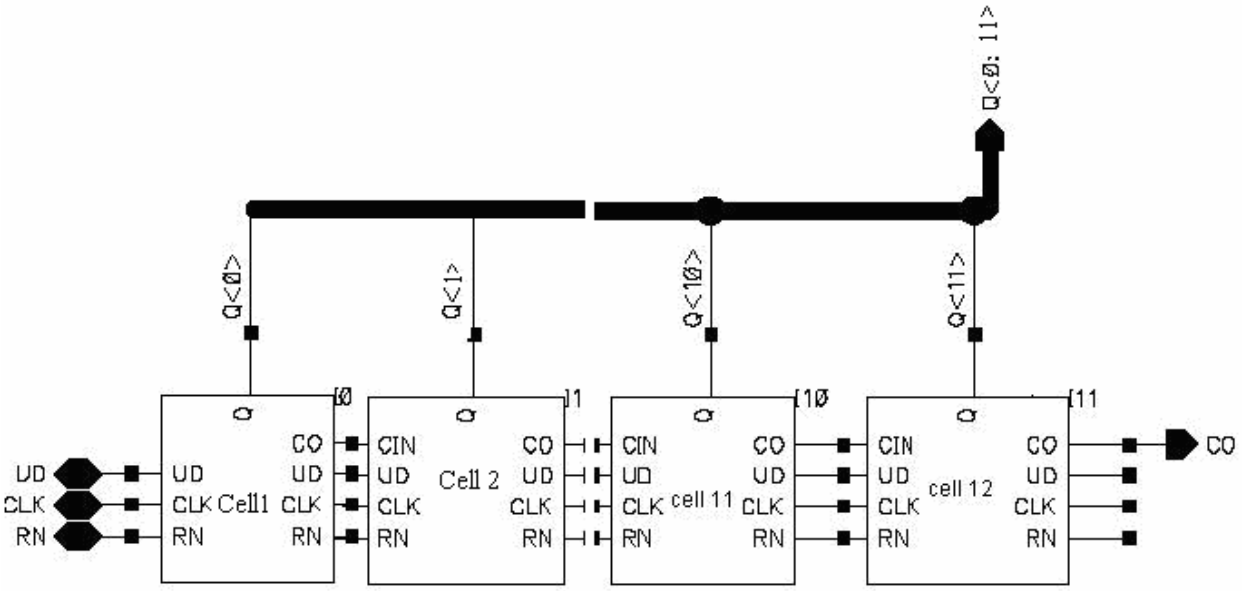

Figure 4.11: *Abridged functional block diagram of the counter*

The functional block diagram, as shown in Figure 4.11, shows the counter cells 1, 2, 11 and 12. The output of each cell is available on the Q<0:11> bus and is connected to the shift register.

Figure 4.12 (a) shows the first cell of the counter and Figure 4.12 (b) shows the structure of 11 other identical cells. CO of each cell is connected to the CIN of the next cell. RN is the reset input and UD is the direction input.

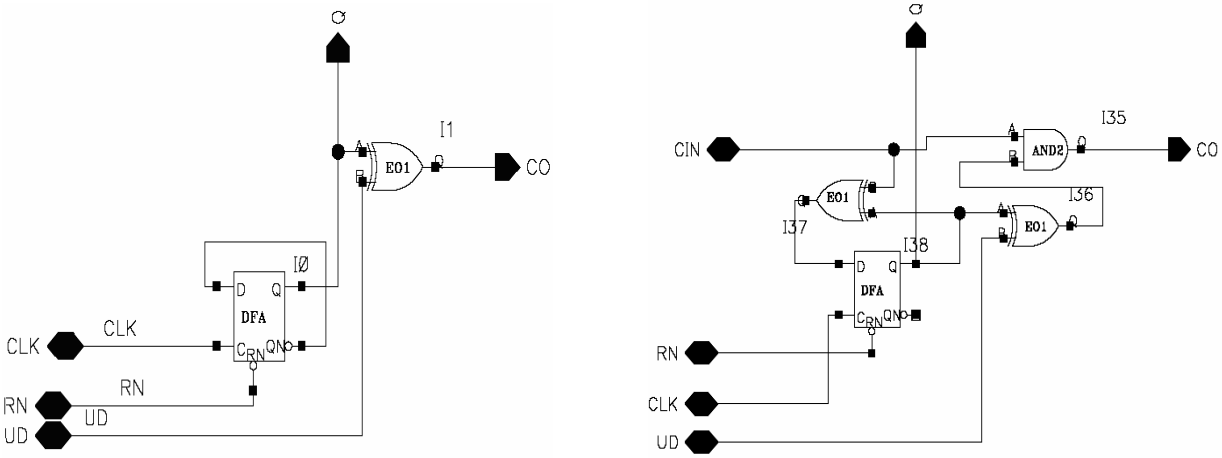

Figure 4.12 (a): *First cell* **Figure4.12 (b):** *11 other cells (identical) of the up/down counter*

The bit-line BLF is buffered and used as the clock for the counter. The counting modality is driven by the signal DIR, which changes the up/down direction, as shown in Figure 4.10, together with the algorithm direction. The number of required bits depends both on the number of pixels (M+1) of the linear sensor and on the desired sub-pixel resolution. The counter is designed with the standard cells and the layout fits in the constraints of pixel pitch.

4.3.3 Shift register

The shift register, as shown in Figure 4.13 (a), is used to shift the data serially. It is composed of 12 identical cells, as shown in Figure 4.13 (b). RESNSR, CKBIN and Qin are the reset, clock, test signal inputs and Qserial is the output of the shift register respectively. Q<0:11> are the inputs to the shift register from the up/down counter. SEL input determines data storage mode (LO) or shift register mode (HI).

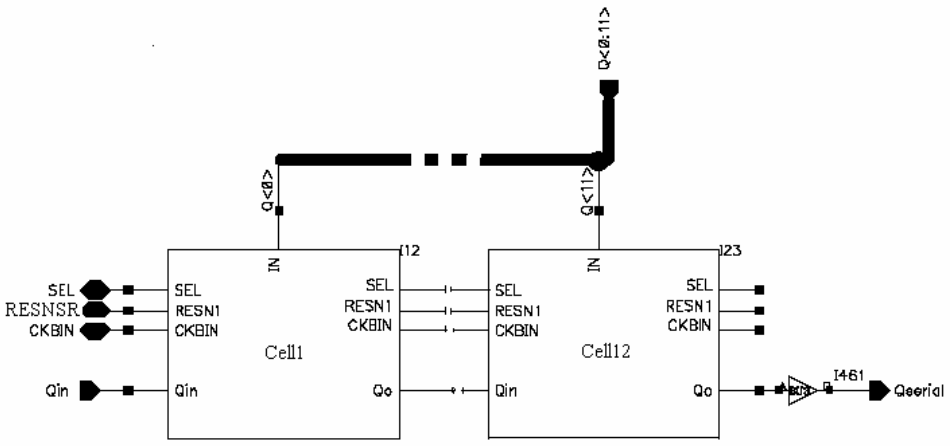

Figure 4.13 (a): *Shift register block diagram showing cell1 and cell12*

During data storage mode, the data from the up/down counter is loaded, in conjunction with the first clock pulse of CKBIN and during the shift register mode, the data is shifted serially in subsequent 11 clock cycles.

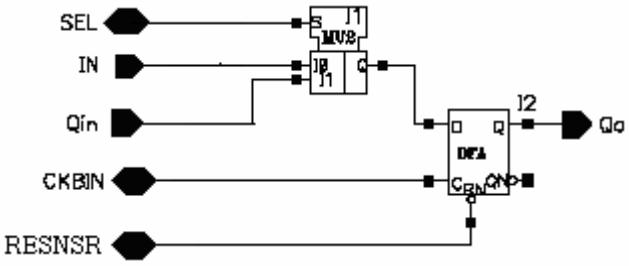

Figure 4.13 (b): *12 identical cells of the shift register from the standard cell library*

4.4 2D Architecture

On the basis of the discussion on the smart linear sensor design so far, the sensor architecture is proposed to be an array of N identical (M +1) pixel smart linear sensors, as shown in Figure 4.14, and each linear sensor implementing a position sensitive device functionality. The output of each linear sensor is available on the corresponding output of the up/down counter. All the outputs connect to the bit bus. This data represents the range information of the object provided in one frame. After one complete cycle of position detection operation, the N final values are stored in the N up/down counters ready to be read out through the n-bit data bus. Each counter is selected by the decoder drives the data bus providing its final value.

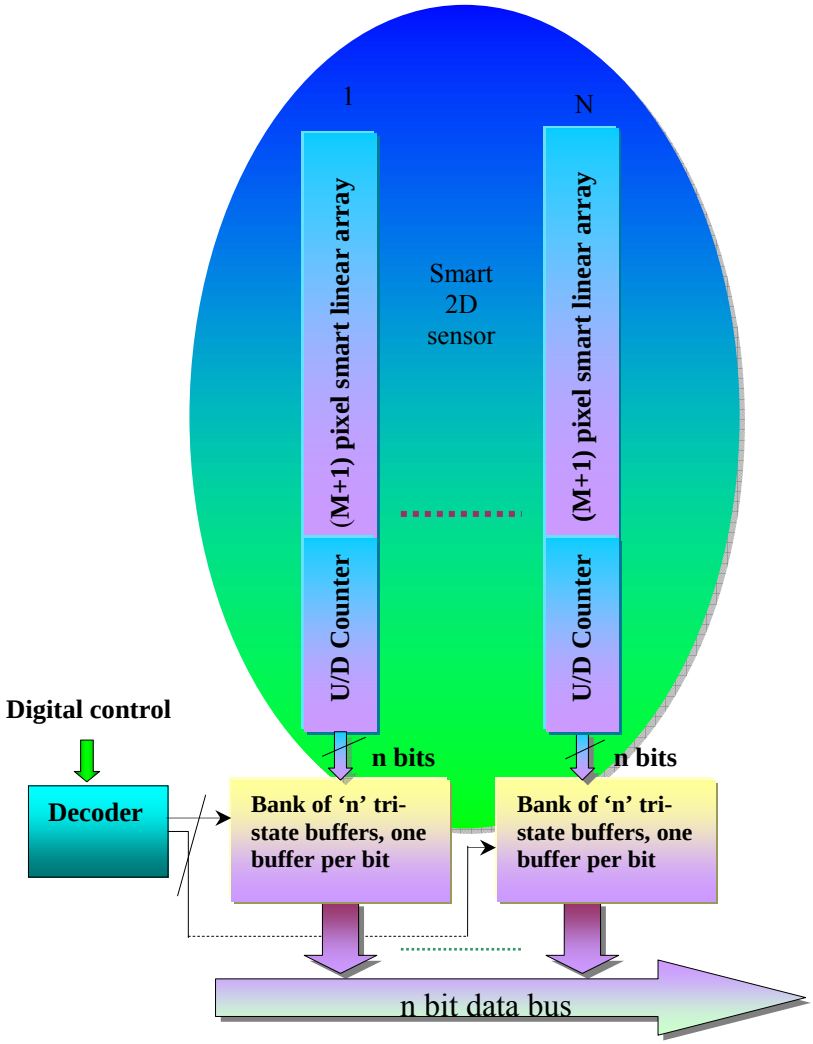

Figure 4.14: *Proposed architecture of the 2D sensor*

Chapter 5
Device Testing

5.1 Introduction

This chapter presents the testing environment and the procedures that have been used to verify the operational characteristics of the image sensor. The device incorporates full testability features for testing each block separately and in combination. The features also are applicable during the system testing with the optical test setup. After describing the electrical testing, the subsequent sections discuss the functional testing of the device with optical bench and logic state analyzer. The last section presents interfacing with FPGA.

The purpose of the testing is to find the performance of the device, estimate the specifications and judge its conformance with the design. The results and analysis are presented in chapter 6. The test features are divided in to electrical testing, logical testing and optical testing. While the electrical test determines the functionality of individual blocks, the logical test executes the testing of the device with external patterns. The individual test features enable isolation of the faults in operational conditions with different blocks. The optical test determines the performance of the device in terms of speed, resolution and accuracy.

5.2 Imager board block diagram

As shown in Figure 5.1, the imager board block diagram illustrates the sensor with its constituents, locations where testability is incorporated. While the pixel array is a mixed mode design, the rest of the device is digital.

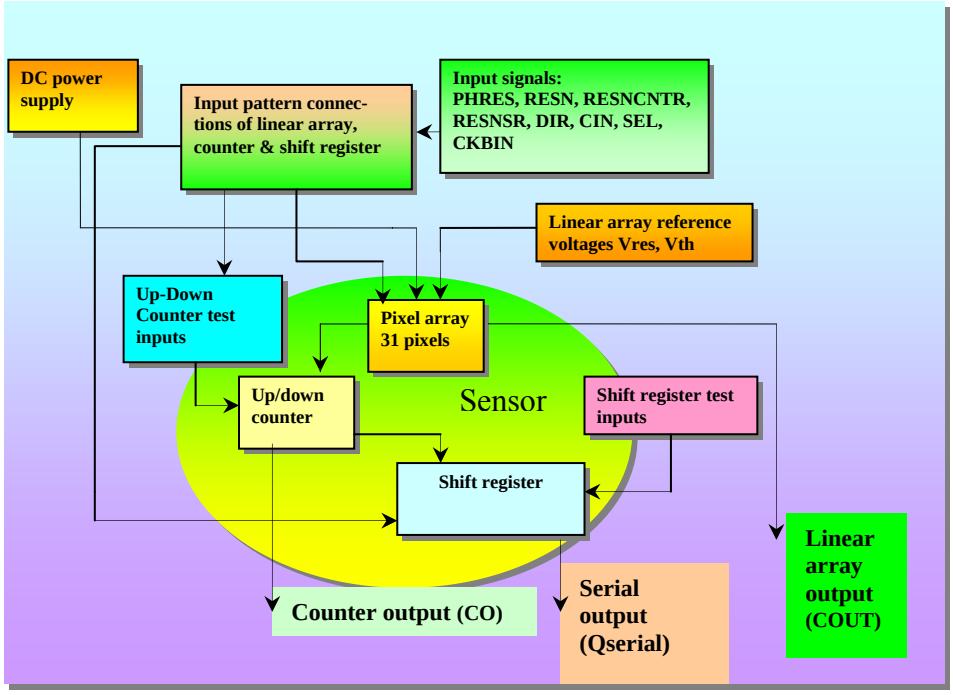

Figure 5.1: *Imager board block diagram*

Since the sensor consists of all the test features, the board merely provides electrical and mechanical support (voltage settings, I/O signal connections and switches) to the device and no other signal processing features are available or needed for the test. The features of the device are tested using an optical bench equipped with a pulsed laser source and precision micrometers in XYZ directions (for the adjustment and movement of the imager board).

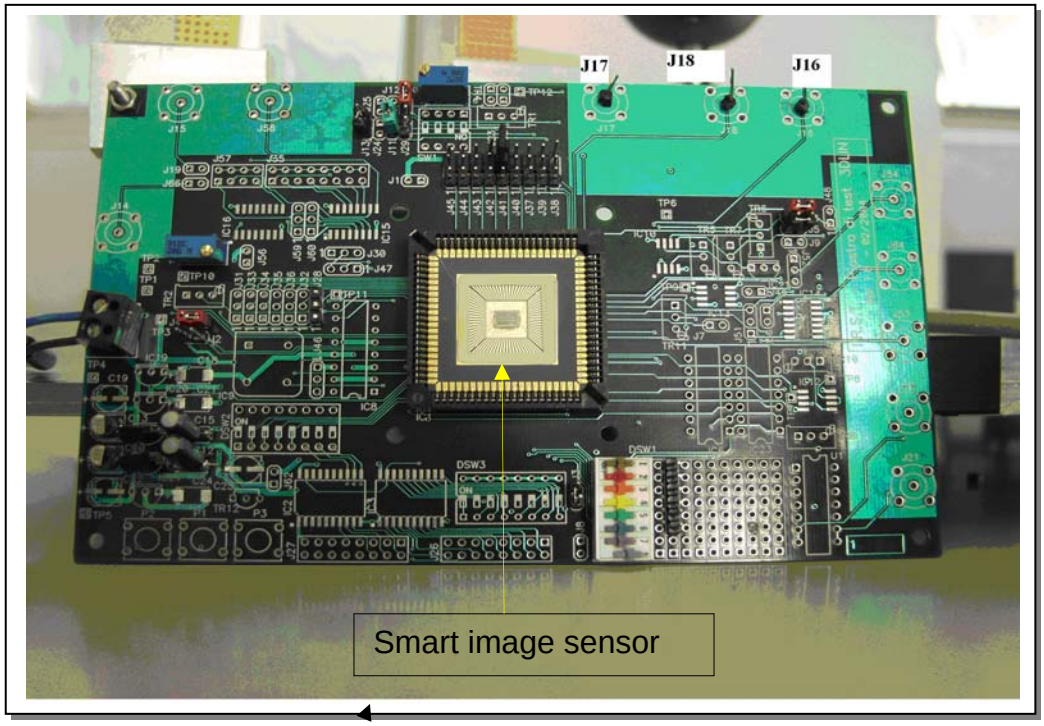

Figure 5.2: *Imager Board*

HP 16500A (for electrical testing) and TEK TLA 714 pattern generator/ Logic analyzer (for subsequent testing), Philips pulse generator and a Xilinx Spartan IIe FPGA based board are used for test pattern generation, data acquisition and interfacing.

The imager board, as shown in Figure 5.2, consists of the test chip, which has a prototype of the linear sensor along with other test devices. The outputs, CO (Up/down counter output), Qserial (Image sensor output), COUT (Linear array output) are available for testing the device.

5.3 Electrical testing of the linear sensor

The electrical test includes testing of individual blocks with external test inputs, estimation of power consumption and timing details. The block diagram, as shown in Figure 5.3, shows the individual blocks of the linear sensor with the interconnections. The signals (Appendix B) include the input signals generated by the test setup, output signals generated by the device, the threshold voltage (V_{th}) and photodiode reset voltage (V_{res}) inputs. The electrical test setup, as shown in Figure 5.4, includes the imager board, a pattern generator and an oscilloscope. A configuration file loaded in the pattern generator enables testing of the blocks.

5.3.1 Testing of functional blocks

The linear array can be tested by the burst of pulses it generates on the forward bit-line (BLF) and the presence or absence of the COUT pulse at its output. The pulses generated on BLF are used as the clock for the up/down counter. BLF is connected to the CLK input of the up-down counter through a multiplexer included for testing purpose. *H* (high) on TSTCNTR enables TSTCLK for testing the counter by feeding it with an external clock and *L* (low) enables the bit-line to be connected to the CLK input, providing burst of pulses to the counter.

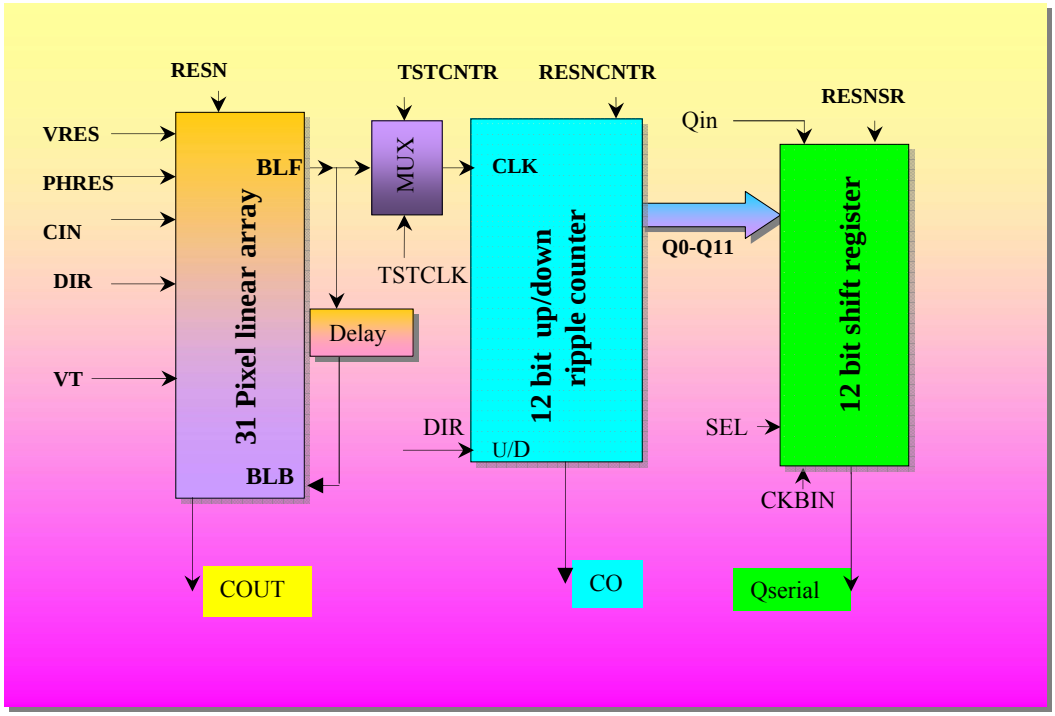

Figure 5.3: *Functional block diagram of the sensor*

Similarly, *H* on SEL enables the shift register mode of operation. A test input on Qin can be used for testing the shift register using CKBIN as the clock. RESN, RESNCNTR and RESNSR are the reset inputs (active low) of the image sensor, up/down counter and the shift register blocks respectively. *L* on SEL triggers the 'load data' mode and enables the counter output to be loaded into the shift register. Thus, all the three blocks can be separately tested.

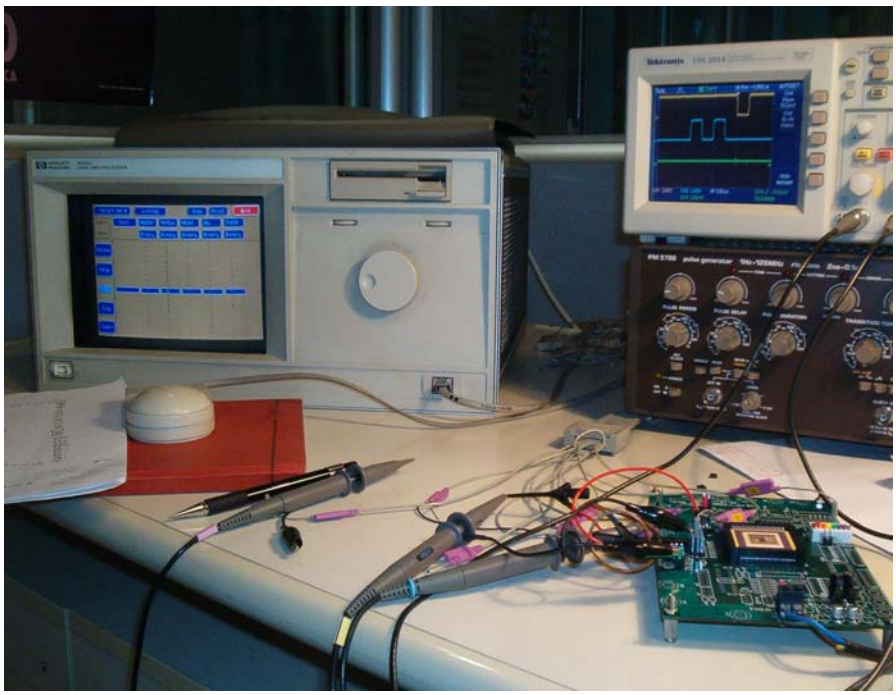

Figure 5.4: *Imager board electrical test setup*

5.3.1.1 Testing of the linear array

This test identifies if the pixels in the array are below or above the threshold voltage by generating corresponding outputs on bit-line and carryout. The test is performed by deactivating (resetting the common PHRES input signal of the photodiodes) the optical input of the array and presetting the threshold and reset voltages to the array. Since it is not possible to address each pixel separately (as can be done during simulation), in the electrical testing the only way to know the effect of the optical input is to directly read out the bit-line and carryout signal.

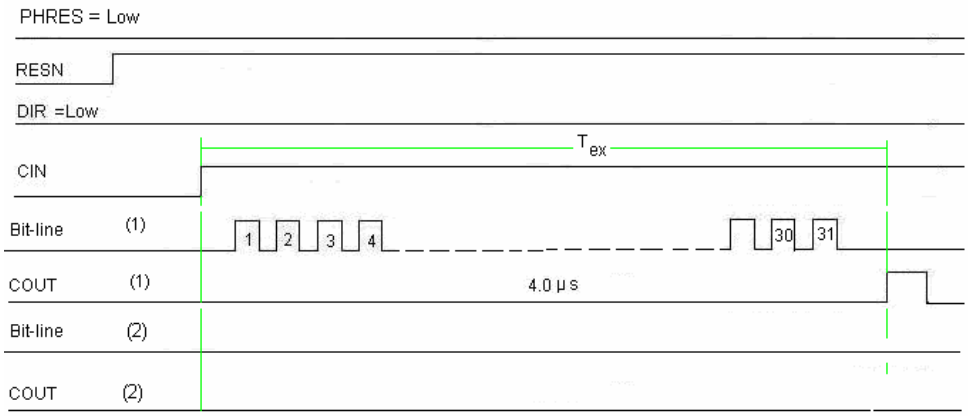

Figure 5.5: *Linear array generating (1) pulse burst and carryout pulse when $V_{res} > V_{th}$ and (2) no pulses on bit-line and no carryout pulse when $V_{res} < V_{th}$*

The test is initiated by a configuration file in accordance with the waveform shown in Figure 5.5. PHRES is permanently set to *L* to disable the photodiodes integrating light, the sensor is taken out of reset state with *H* on RESN and the search in forward direction is initiated with *H* on CIN and *L* on DIR, realising :

(i) As shown in Figure 5.5(1), a burst of 31 pulses on the bit-line in forward direction when $V_{res} > V_{th}$ and the carryout signal on COUT, and

(ii) No pulses, as shown in Figure 5.5(2), on bit line and COUT, when $V_{res} < V_{th}$. Since all the pixels receive the same reference voltage through V_{res}, when the first pixel crosses the threshold, the carryout pulse does not propagate and no pulses will be available on the bit-line.

A similar result is observed when DIR is *H*, showing the search process in the reverse direction.

Recalling the equation 4.1, $T_{exm} = (M+1)\,\tau$, the time taken to complete the search process in one direction is found to be 4 µs for 31 pixels. Since one operating cycle consists of computation in both directions, the total execution time is 8 µs. This is an important parameter of the linear array conforming to the simulated value and useful in making the measurement for testing the device in optical setup.

5.3.1.2 Testing of up/down counter and shift register

The counter and the shift register are initially reset and released. DIR and SEL are set to *L* indicating forward direction and the storage mode of shift register, respectively. Input on TSTCLK provides the number of pulses the counter has to count. CKBIN, the clock of the shift register should be enabled before the transition from storage mode to shift register mode. This causes the transfer of all the counter outputs, in parallel, in one clock cycle to the shift register. The SEL is now set *H* showing the shift register mode of operation. After the single clock pulse, which facilitates the data transfer, the next 11 pulses of the CKBIN shift the data. The same can be continued for reverse direction setting *H* on DIR. The resultant output at the Qserial will be zero, nullifying the outputs of forward and reverse directions. The CLK replaces the TSTCLK input of the counter when using the device as imager. The pulses are counted in forward and reverse directions by incrementing and decrementing the counter and the result is output to the

shift register through the Q0 to Q11 bits in parallel. Initially the shift register is in storage mode (SEL=0). TSTCLK is applied with 5 pulses in forward direction and 4 pulses in the reverse direction. At the first pulse of CKBIN, the data available in the counter (5-4=1) is loaded to shift register and when SEL=1, the data is shifted serially and the result can be observed on Qseiral.

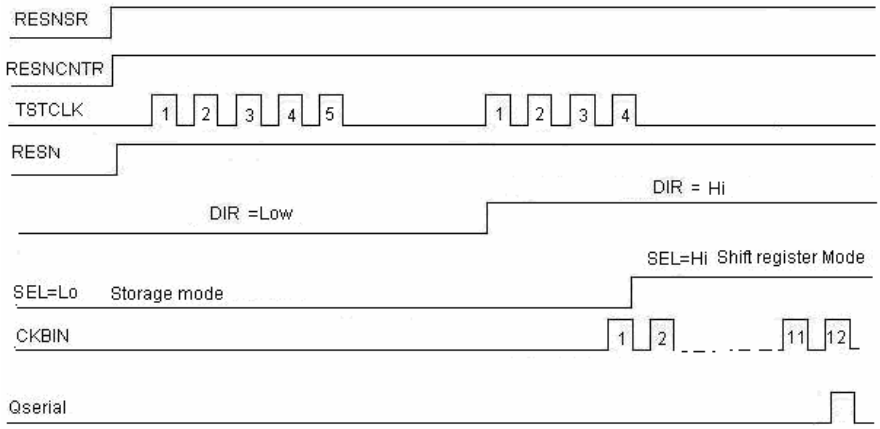

Figure 5.6: *Shift register and up/down counter test: Serial data output on Qserial*

5.3.2 Linear sensor testing

After testing the linear array, the counter and the shift register, all the three blocks are tested together. In the sensor testing, it is expected that when $V_{res}>V_{th}$, no pixel crosses the threshold generating 31 pulses in one direction and the carryout pulse is generated. With $V_{res}<V_{th}$, all pixels cross the threshold. Since the computation is identical in both directions, Qserial should be zero in both the cases.

As shown in Figure 5.3, initially all the functional blocks are reset and released. The photodiode is permanently reset with *L* on PHRES since the light interaction is not being considered in this part. With *L* on DIR, *H* on CIN initiates the search in forward direction. The CIN high pulse should be >4 µs to give time for the completion of the search process in up and down directions for the 31 pixels at100ns clock, as explained earlier. *L* on TSTCLK enables the counter to read the output of linear array.

With the first pulse of CKBIN, and L on SEL, the data available in the counter is loaded in to the shift register. When SEL is *H*, the data is shifted serially during the remaining 11 pulses of CKBIN. Figure 5.7 shows the I/ O waveforms.

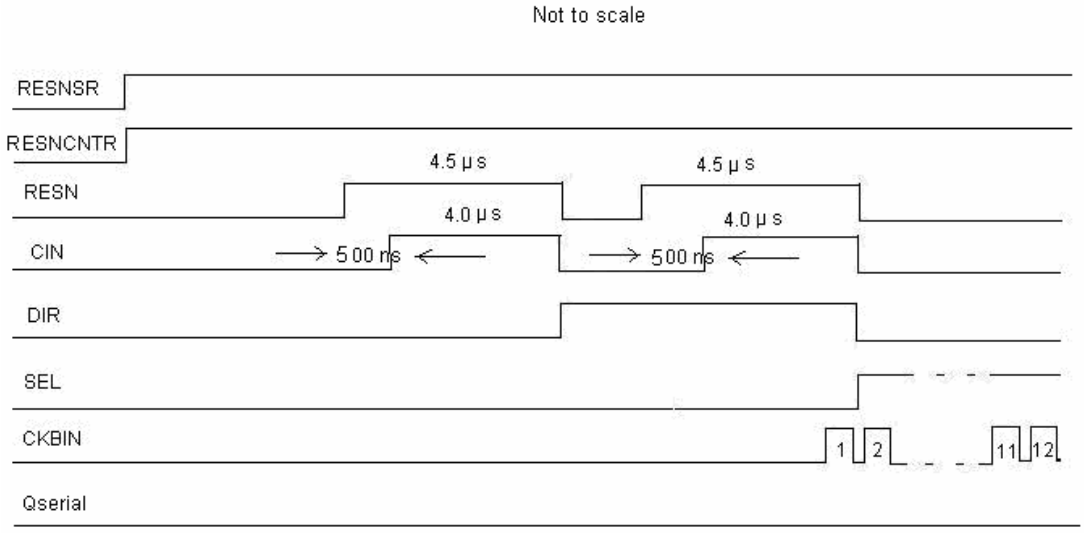

Figure 5.7: *Q serial after one operating cycle*

The next section describes the device testing with the optical setup.

5.4 Optical bench & pattern generator test setup

The purpose of this test is to take measurements for finding the position and shape of the reflected laser spot. As shown in Figure 5.8, the setup consists of the imager board, a laser source, TEK TLA714 logic state analyzer/pattern generator etc. Micrometers 1-3 are used for XYZ motion of the imager board and micrometer M4 is used for moving the laser source to project a spot on a plain surface. The reflected light, being collected by the imager, is defocused with a lens to spread the distribution about 7 pixels. This enables the measurements for estimating the resolution and accuracy of the device. The pattern generator provides the proper digital control signals through the configuration files and connects to the imager board through its pod. It also provides the signal to the function generator for driving the laser.

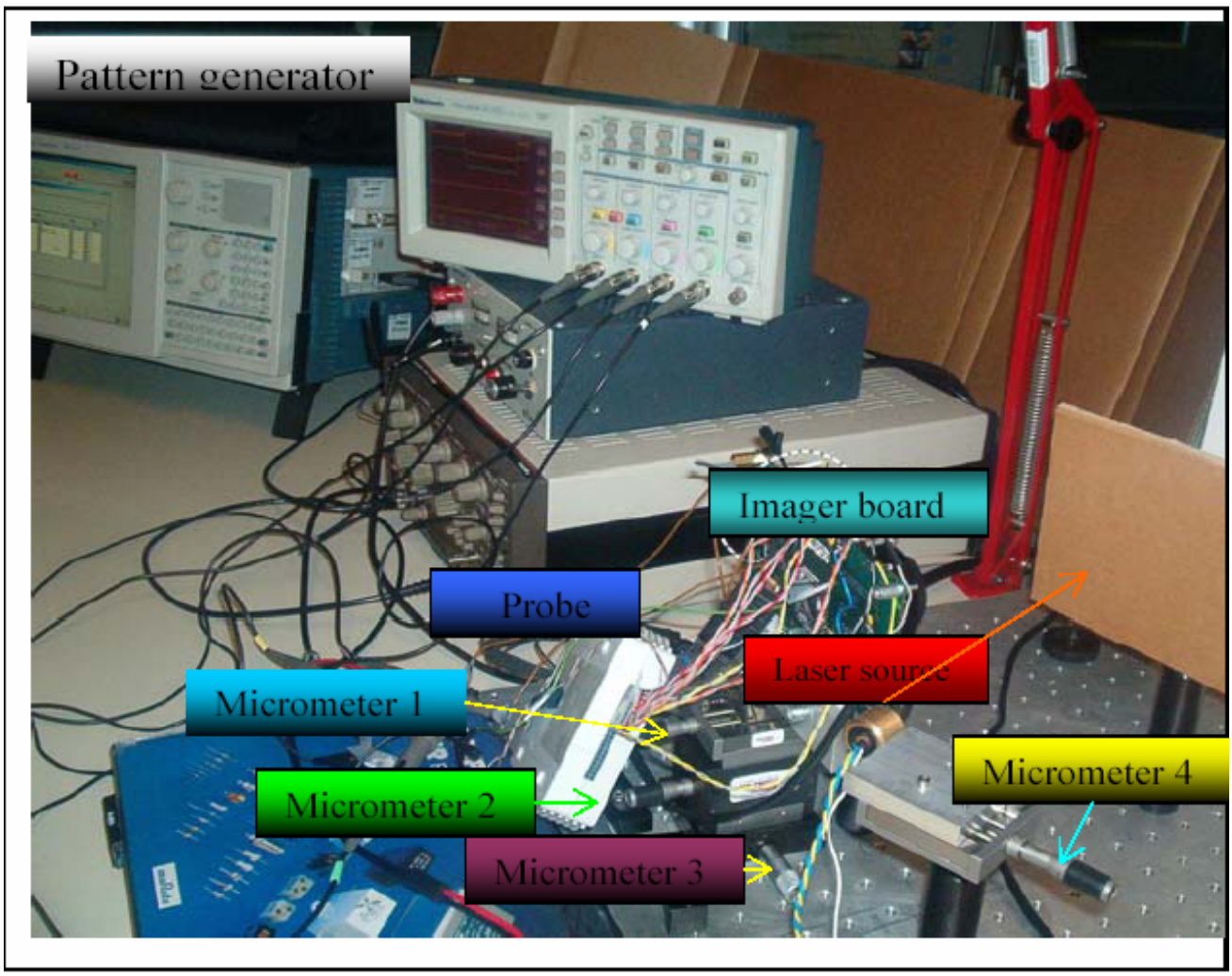

Figure 5.8: *Imager board testing using optical test setup*

Two configuration files are made viz., (i) up/down counting together and (ii) up/down counting separate. While the former gives the effective pixel value of the up-down counting and is used in multiple images binarization (as explained in chapter 3), the latter gives the up and down count values separately and is used for estimating the spot shape.

5.4.1 Measurements for multiple images binarization

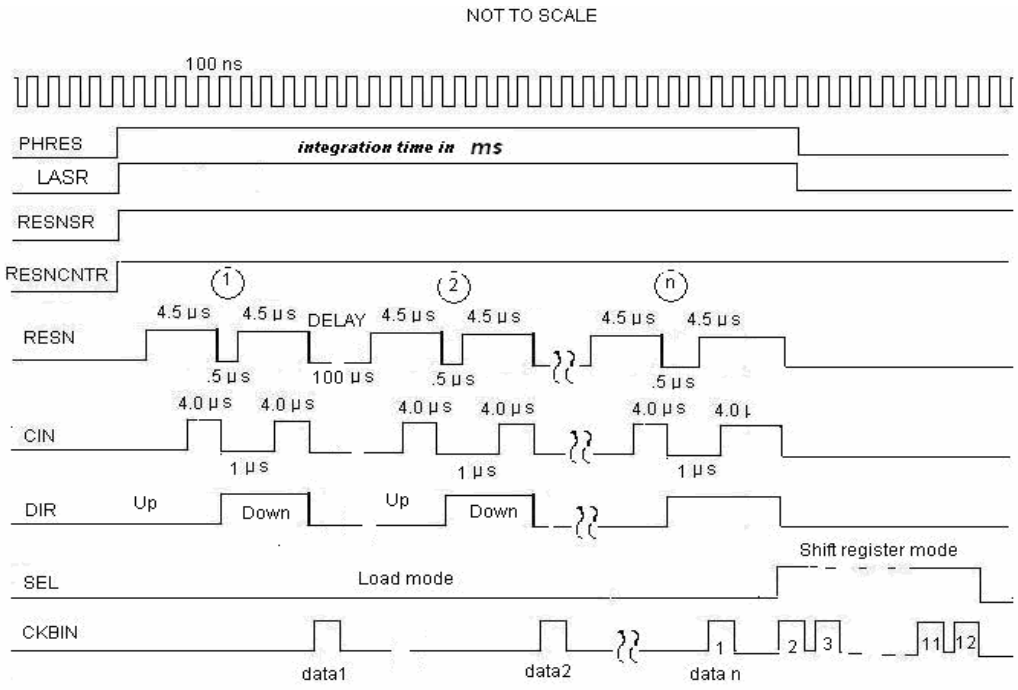

Figure 5.9: *Overlapping image acquisition with image processing*

The configuration file for taking the measurements for spot position follows the waveform pattern shown in Figure 5.9. V_{th} and V_{res} are fixed at 1.5V and 2.0 V respectively. While the multiple thresholding operations (as mentioned in Chapter 3) are performed after the integration period, in the multiple images binarization, the image processing is run during the image acquisition.

With the increasing integration time, more and more pixels participate in the search process. After crossing a preset threshold voltage, the search process starts collecting the centroid values. As shown in Figure 5.9, during the integration period, a number of up and down operations are performed, with a uniformly spread delay value after every successive up/down cycle, and measurements are taken. In each operation, the centroid is estimated and the value is accumulated in the counter. After all the operating cycles are concluded (one loop), SEL becomes *H* and the data is shifted by the shift register in the subsequent 11 cycles of CKBIN. In this way, by moving the laser spot position with the micrometer, multiple measurements are taken along the length of the sensor. This leads to an important discussion of the thesis on determining sub-pixel resolution with the multiple measurements, obtained during the integration time for a particular position. The results are analysed in Chapter 6.

5.6 Imager interface with FPGA

The imager interface with FPGA provides an integrated and compact test environment to test the imager. While replacing the pattern generator, this interface also shows flexibility in data processing. The test setup, as shown in Figure 5.11, consists of a Xilinx Spartan IIE FPGA board [MEM] with JTAG and serial interfaces and a P160 expansion slot. The FPGA board provides input signals to the imager board and the laser source through the expansion slot, and transfers data to the PC through serial interface. The PC programs the FPGA through the JTAG interface.

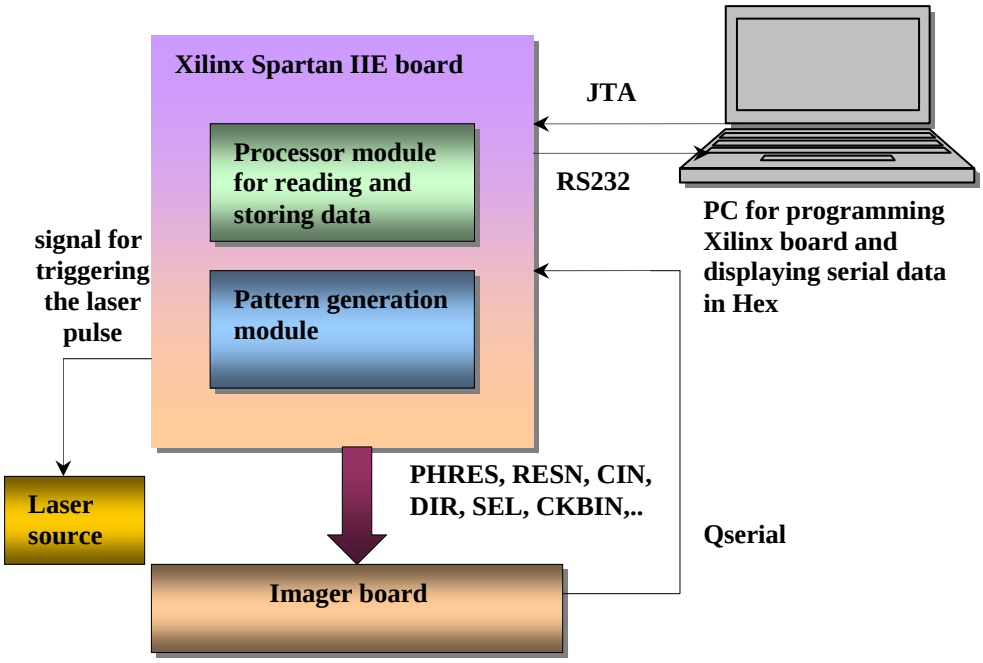

Figure 5.11: *Imager testing in Spartan IIE environment*

Two methods of image acquisition and processing are proposed with this setup. *Image binarization after integration*, as shown in Figure 5.12 (a), where the search process starts after the integration period and *image acquisition during integration*, as shown in Figure 5.12 (b), where the search process starts during the integration period. The input signals viz., PHRES, LASR, RESN, RESNCNTR, RESNSR, CIN, DIR, SEL etc., are generated by VHDL code, which is based on the state machine behaviour, as shown in Figure 5.13.

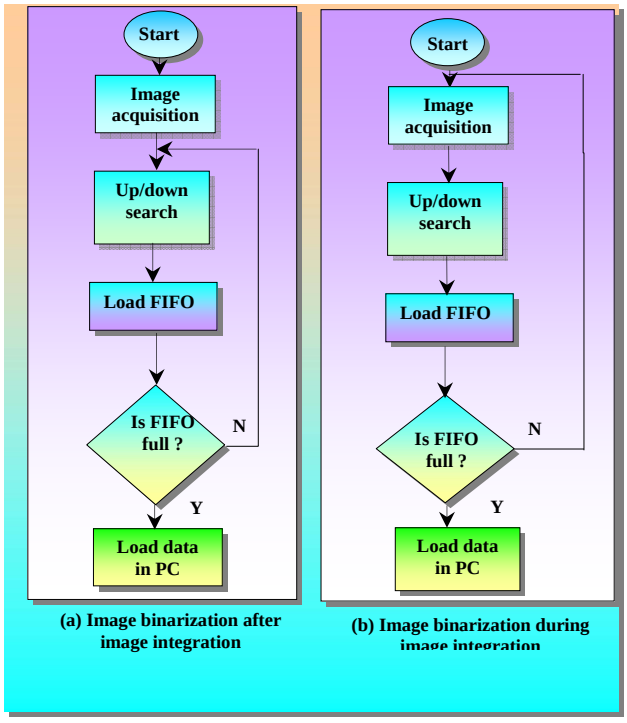

Figure 5.12: *Two cases of image binarization*

5.6.1. Image binarization after the image integration period

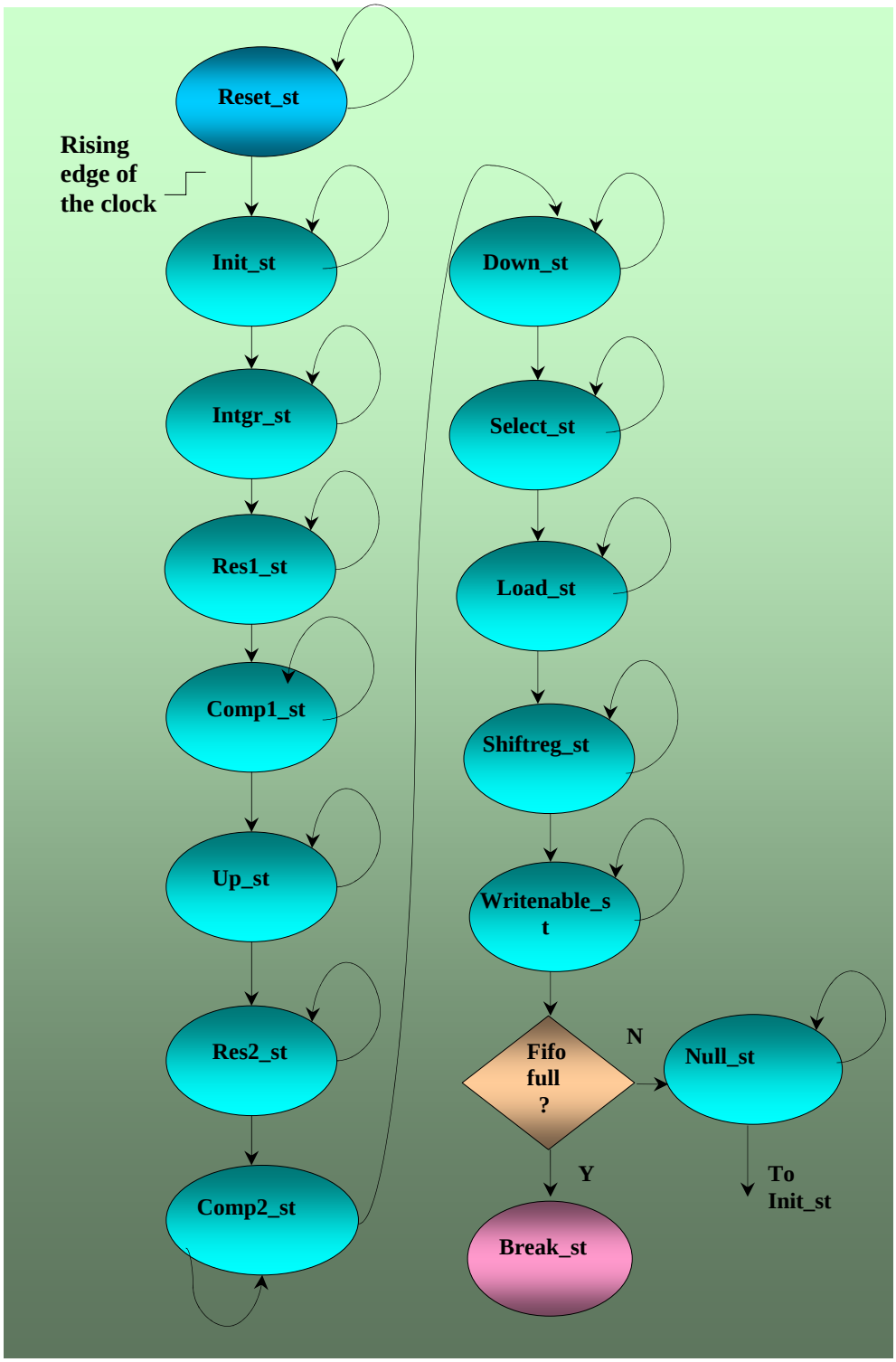

Figure 5.13: *State diagram showing transitions*

The different states are defined according to the timing shown in the Figure 5.14. Initially, the process is in Reset_st, with all the signals are at low value. When the reset is disabled, at the rising edge of the clock the state machine takes control of the execution of the program.

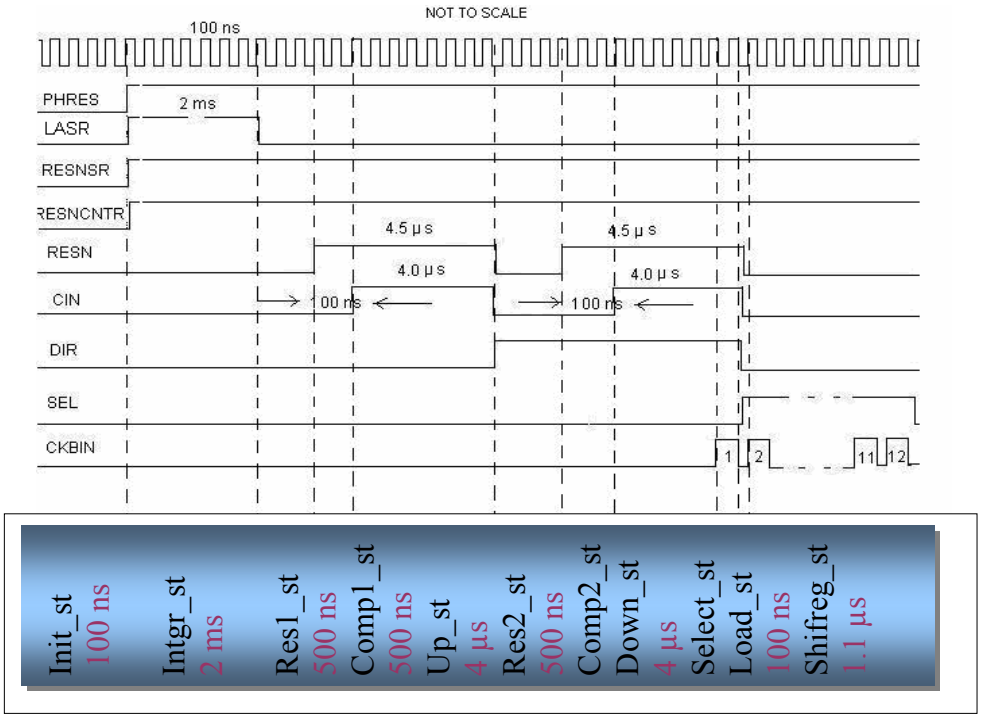

Figure 5.14: *Waveforms and states of the corresponding FSM with timing consideration*

Whenever there is a change in any of the signal behaviour, a new state occurs. During Init_st, all the input signals are set to low value. In the Intgr_st, the PHRES, LASR are high, the counter and the shift registers are activated. The imager starts integrating the light. During the Res1_st, the laser is turned off. This completes the image integration process. During the Comp1_st, the sensor is brought out of reset state, with RESN set high. During the Up_st, CIN is *H* initiating the forward search. In Res2_st, CIN is turned off along with RESN. In Comp2_st, the sensor is out of reset with *H* on RESN. CIN is turned on again along with DIR to commence the reverse search in Down_st. In Select_st, the clk_enable signal is set high to initiate the shift register clock (CKBIN) during the next state. Clk_enable signal selects either the reference clock or a low signal (0), which are multiplexed to generate the CKBIN signal. At the immediate rising edge of the reference clock, CKBIN is set high during the Load_st and the data from the counter is loaded in to the shift register. The clk_enable remains high until the end of the Shiftreg_st. During the Shiftreg_st, SEL is high, enabling the shift register mode of operation.

In addition to the above-mentioned states, three more states are defined for the execution of the program. They are Null_st, Writenable_st and Break_st. During the Null_st, all the signals are brought back to zero. Additionally, the FIFOFULL flag of the FPGA is checked continuously in every state, except in the single clock period states, viz., Init_st, Null_st, Load_st and select_st. During these states, the process automatically moves to the next immediate state. If the FIFO is full, the state immediately terminates to Break_st. If not, it continues in the same state until its timing constraint is met and moves to next state. In the Writenable_st, the Writenable signal is set high enabling the data to be written into the FIFO of the FPGA. If the FIFO is full, the state immediately terminates to Break_st. Otherwise it jumps to Init_st via the Null_st, and another operating cycle starts.

5.6.2 Overlapping image acquisition and processing

The multiple images binarization is addressed by overlapping the image acquisition and processing instances. Figure 5.15 shows the timing sequence of this case. By creating a counter with the required number of loops and executing the program during the integration time until all the loops are exhausted, one can obtain the readings for sub -pixel resolution.

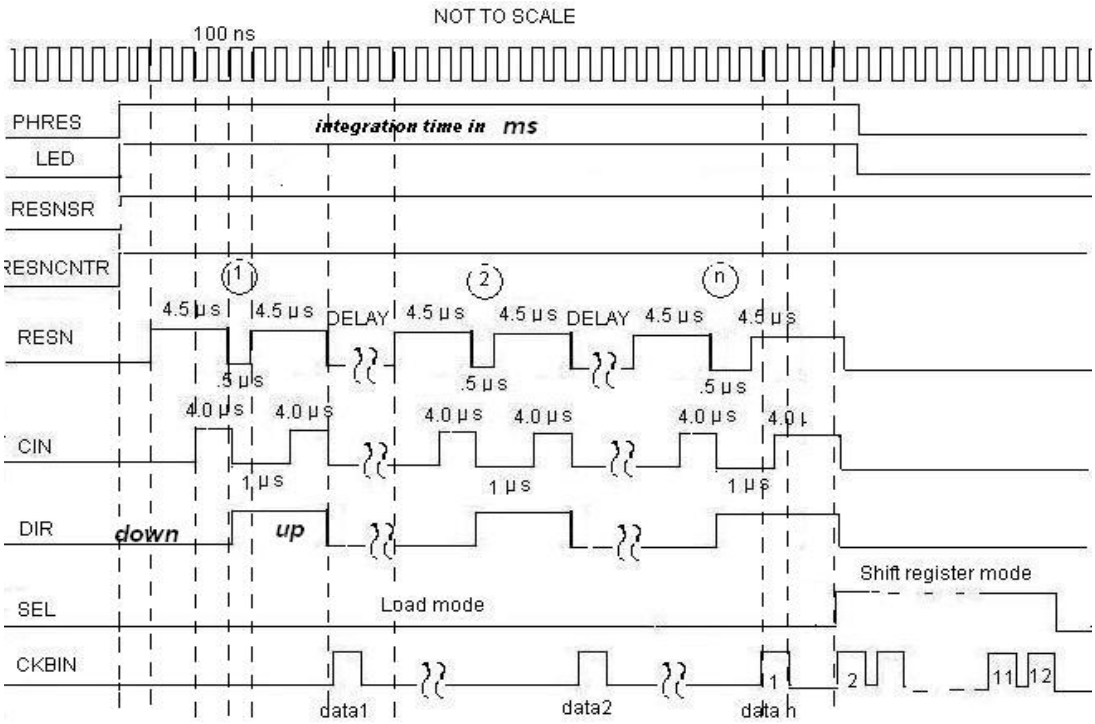

Figure 5.15: *Overlapping image acquisition and processing*

Figure 5.16 shows the practical setup of the imager testing and the serial data (centroids information) received from the imager being displayed in hex.

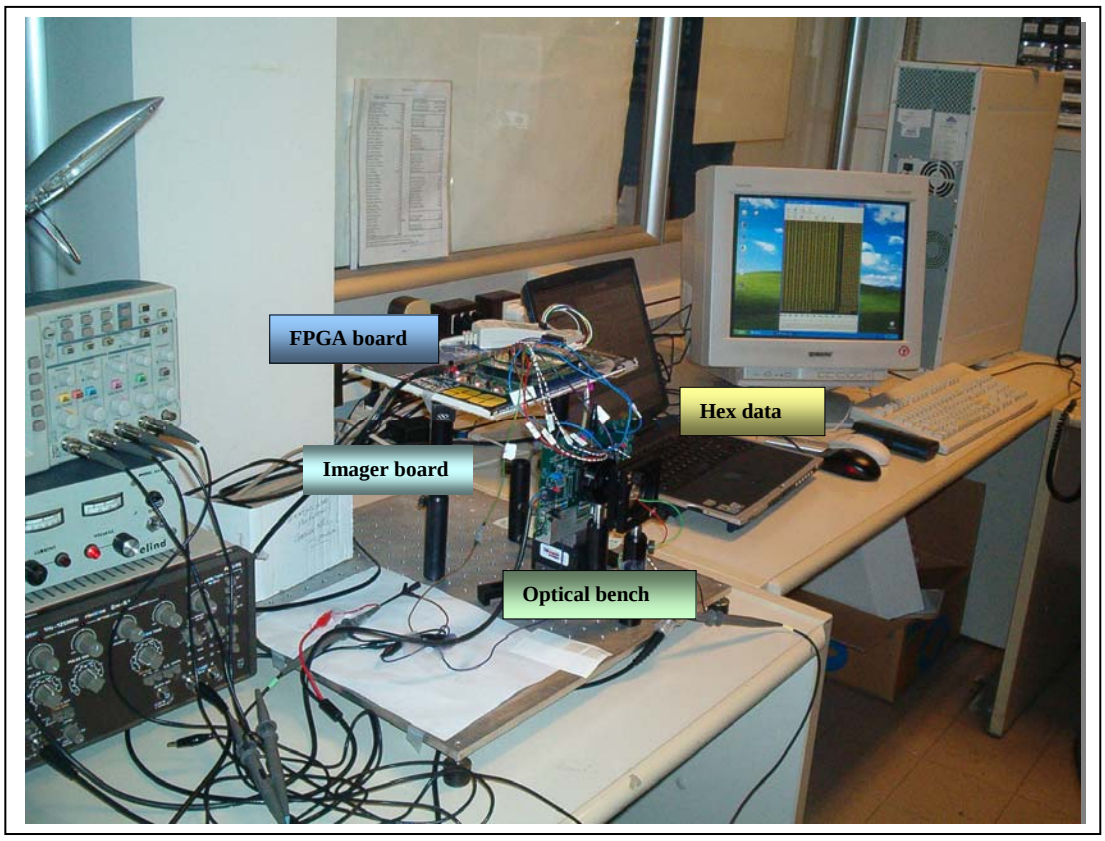

Figure 5.16: *Imager testing with FPGA setup*

The advantage with the FPGA interface compared with the pattern generator method is that the setup is compact, programmable, substitutes for the pattern generator functionality and the serial binary output data is directly available on the PC.

5.6.3 Integration time vs. process cycle time

While the minimum integration time is 18 ms, the process cycle time (for the forward and reverse search operations and outputting serial data) is only 11 µs. Hence, 128 different operating cycles consisting (of up/down search processes), with sufficient delay (100 µs) between successive operations can be uniformly distributed in one integration cycle, i.e., 128 x (11+100) µs.

The above mentioned expression also identifies the bounds the computation. If higher loop value is to be considered, it should fall within the integration time period in the existing setup, with the low power laser used in the measurements. Precisely, for Ti =18 ms, a maximum of 256 operations can be performed. Beyond 256, For example, if the Loop value is 512 operations, the counter needs be larger or the pixel propagation needs to be smaller, meaning compacting the pixel.

The measurements carried out using the test setup, as discussed in this chapter, are presented and analyzed in the next chapter.

Chapter 6

Measurements and experimental results

6.1 Introduction

This chapter presents the measurements and the experimental results on the performance of the image sensor. The measurements taken with the imager have enabled the estimation of the position of the reflected light spot and its shape. The statistical analysis of the data discusses the accuracy, resolution and frame rate of the imager.

6.2 Measurement setup

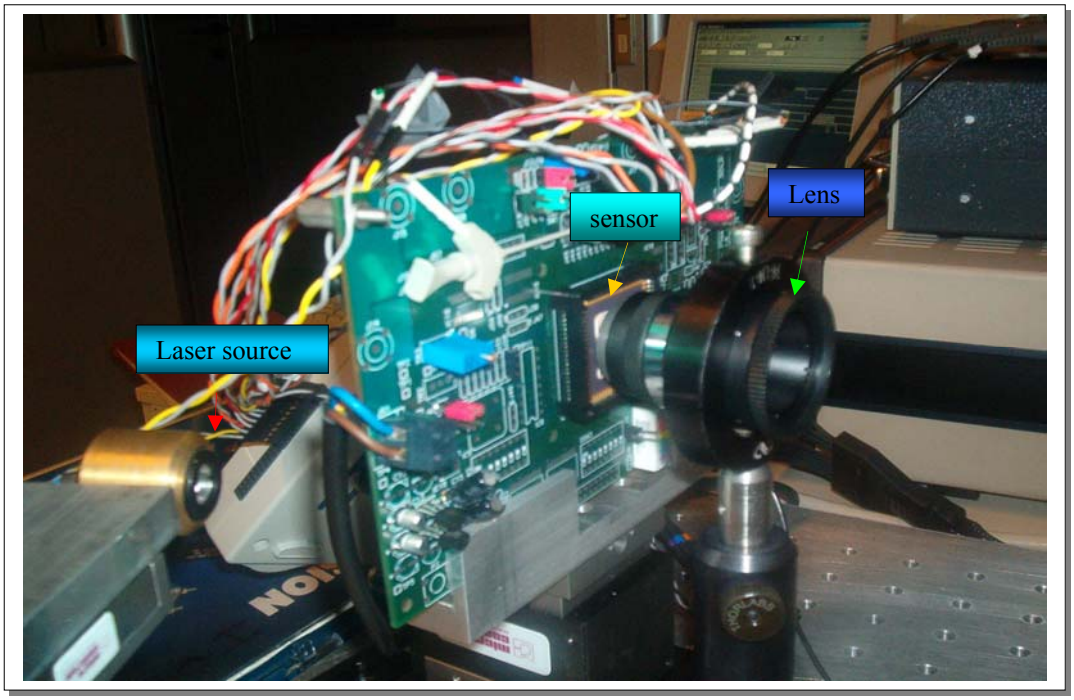

Figure 6.1: *Imager board and lens with laser source*

Before taking the measurements, the device response to the ambient light is verified. This is done by turning off the light source and increasing the integration time until a pixel crossing the threshold. After T_{iAMB}= 200 ms, a pixel is seen crossing the threshold, meaning discharging the pixel by 0.5V ($V_{res} - V_{th}$). With the laser source, the value obtained is T_{iLASR} =18 ms. Since, we cannot assume least interference by the ambient light even below $T_{iAMB,}$ the experimental setup was properly covered to ensure minimum effect by the ambient light.

Figure 6.1 shows the measurement setup in which the image sensor receives the reflected light through the lens. As explained in the previous chapter, the imager board and the laser source can be aligned with the micrometers M1-M4. The configuration file, as shown in Figure 6.2, with the required waveform specifications drives the imager for generating the Qserial (the serial output). The sequence of operations consists of Reset, Delay, Loop (Up/Down search process) and Shiftout blocks, with their respective settings to be used in multiple binarization experiment for estimating the sub-pixel resolution. These blocks program the waveforms of PHRES (image acquisition signal), LASR (Laser pulse-integration time), RESN (sensor reset), DIR (direction of computation), CIN (commencement of computation), SEL (load data mode or shift register mode) and CKBIN (shift register clock).

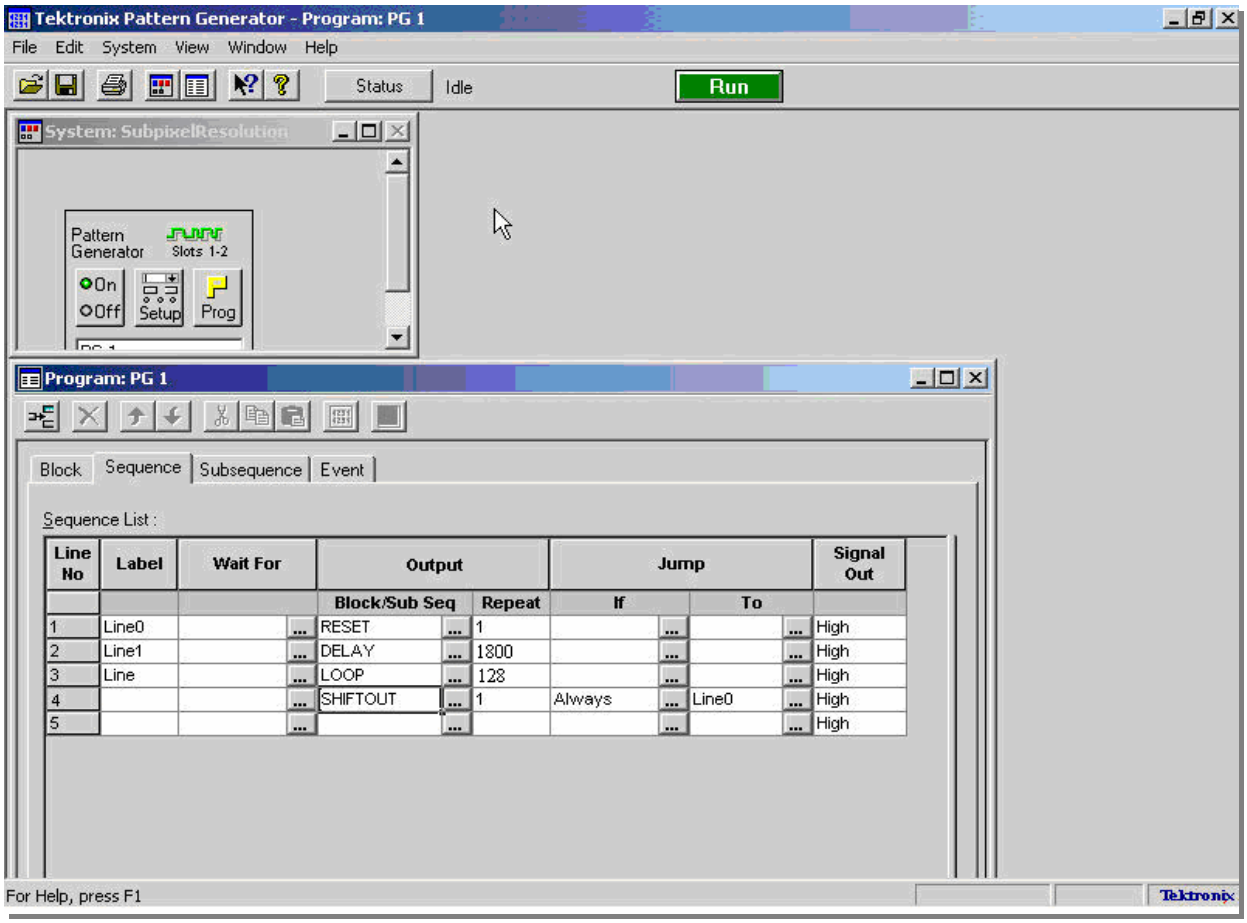

Figure 6.2: A typical c*onfiguration file showing the values of different blocks*

Each block size is defined in a different panel, which identifies the length of the operation, the block has to perform. For example, if a block is set with a value 40, its length will be 4 µsec, when the clock is 100 ns. The delay block shows the integration period which is 18 ms. The loop block identifies the number of operating cycles performing up and down operations. There are sub-sequences, which define the delay between the operations. The execution of the pattern generation file enables the logic analysis panel, which is shown in Figure 6.3.

6.3 Measurements

Two types of measurements are taken. Translating the spot position by moving the laser source (at a fixed imager board position), the imager collects the reflected spot across its length covered by a few pixels. Table B.1 (Appendix B) gives experimental readings to find out position accuracy, which consists of the pixel number, its position in binary, binary to decimal converted value, sub-pixel resolution (achieved by dividing the pixel position with the number of operations carried out) and the difference of successive positions. The binary value is 12 bits, starting from left with the MSB. The 12 bits signify the pixel number followed by the accuracy to the order specified by the number of operations undertaken.

The waveforms in Figure 6.3 (a) and (b) show a sample of sub-pixel resolution measurement. The pixel is 4 (binary 100) and the resolution in sub-pixel region is represented by 8 lower order bits as shown in the figure. Several readings taken over the length of the pixel array enable the accurate determination of the spot position, which is spread over a few pixels, within a few microns, as discussed in the analysis. The

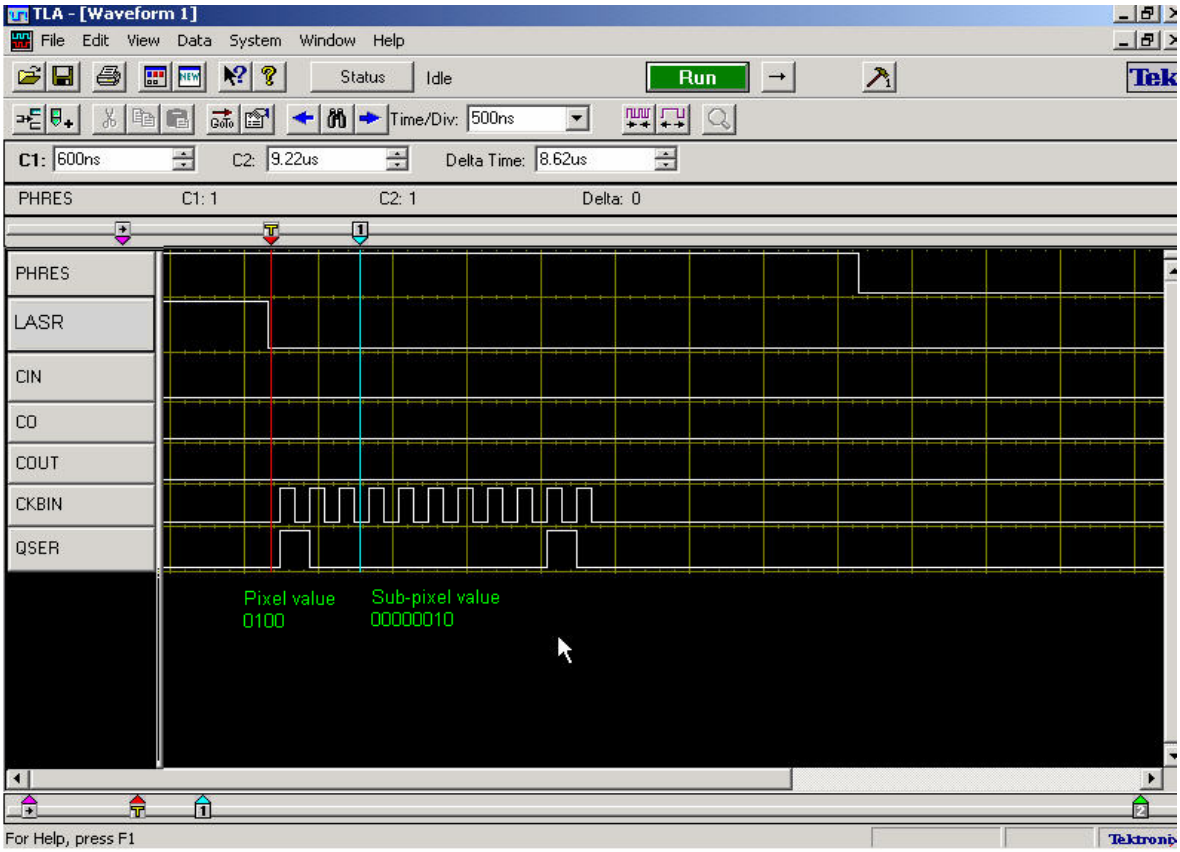

Figure 6.3 (a): *An instance of sub-pixel resolution measurement after integration time*

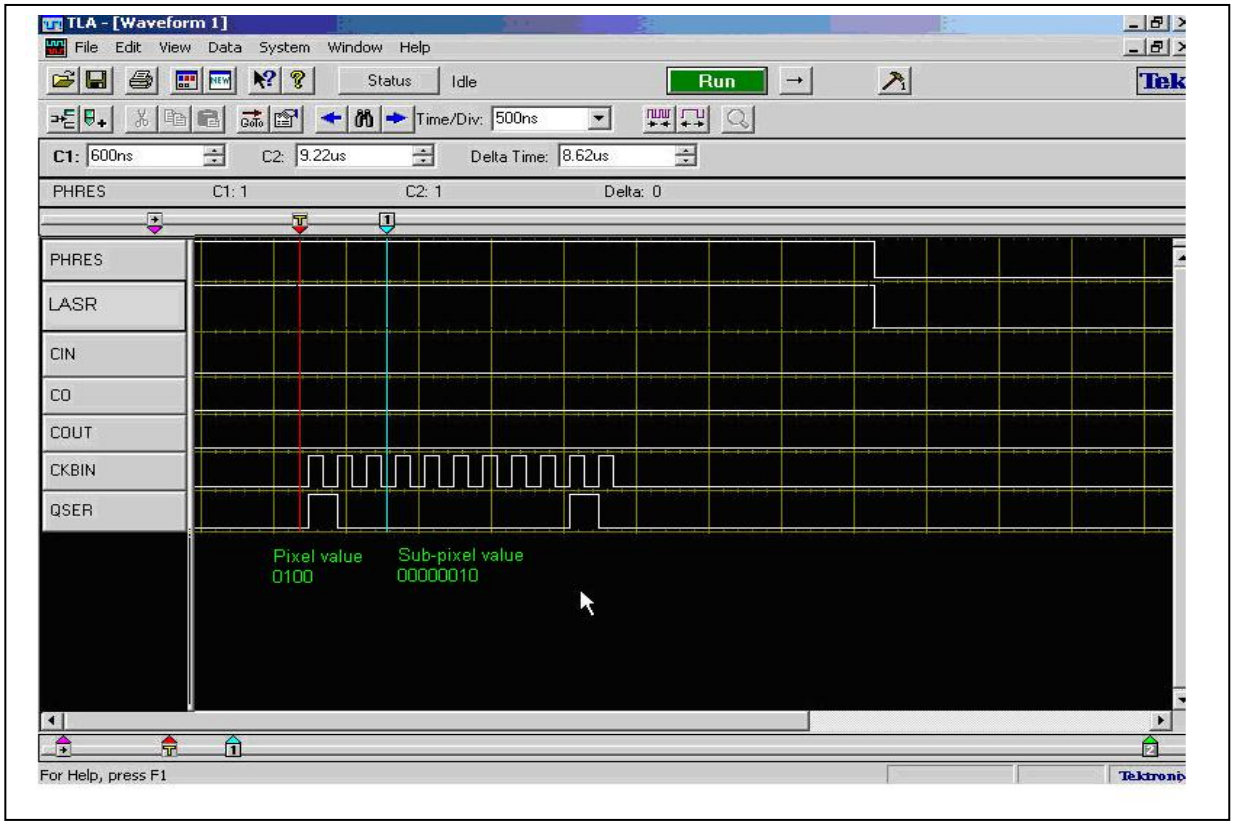

Figure 6.3 (b): *An instance of sub-pixel resolution measurement during integration time*

For example, dividing the bin2dec value by 2^2 gives 1 bit accuracy and the remaining 11 bits give the pixel index. Similarly dividing the bin2dec value by 2^8 gives the 7 bits accuracy, for the 128 operations carried out in one operating cycle. In order to utilise maximum bits for the sub pixel value, the measurements are taken from pixel 1 to 3 (which needs just 2 bits). Due to the relatively higher precision of the experimental setup (0.56 μm) and the large scale factor (18), more measurements can be collected in the 2 pixel interval. This also enables to utilize maximum number of bits available for the calculation of sub-pixel resolution. Hence, the remaining 8 bits of the counter are used to estimate the sub-pixel resolution.

Thus, by dividing with 256, for the 128 operations in one processing cycle, the column div/256 column shows the pixel number followed by its estimated position to the accuracy of 9 decimal points. The column 'difference' shows the difference between successive pixel position values.

Measurements are also taken with the 256 operations. Due to the order of precision obtained with 128 operations, it is concluded that measurements with higher loop value is not required due to very precise nature of the calculations. However, there will be a practical limit in the calculations with the existing setup (due to laser power and counter size, as explained previously), if 512operations or beyond to be performed.

The scale factor of the system is calculated to be around 18 times as 1.6 mm of the shift of the spot position corresponds to 2 pixel pitch.

6.4 Analysis

Statistical analysis of the data presented in this section describes the calculation of the standard deviation, accuracy, INL (Integral non-linearity) and DNL (Differential non-linearity) parameters of the imager.

6.4.1 Standard deviation

The following formula gives the **standard deviation** of the difference in successive positions of 168 (n) values:

$$\sigma = \frac{\sqrt{\sum (x - x_{mean})^2}}{(n-1)} = 0.032978994 \text{ of pixel}$$

which indicates that on the average, the successive measurements differ from the mean by 0.033 of pixel.

(Where *x* is the measurement value as shown in the *difference* column, *x mean* is the mean of the difference column and *n* is the number of measurements.)

6.4.2 Accuracy

Accuracy or error of the measurement is generally stated as $\pm 1\sigma$.

1σ = pixel pitch * standard deviation
= 45 μm x 0.032978994
= 1.484054717 μm ~ 1.48 μm

$\pm 1\sigma$ = 2 x 1.484054717 μm =2.968109434 μm ~ 3 μm

This implies that the sensor has 4bits accuracy (pixel pitch / accuracy).

The scale factor of the system is calculated to be around 18 times as 1.6 mm of the shift of the spot position corresponds to 2 pixel pitch.

6.4.1 Integral non-linearity (INL)

Integral non-linearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the centre of the quantization band.

The integral non-linearity curve, as shown in Figure 6.5, gives relationship between the successive pixel positions, with sub-pixel resolution. A trend line shows the ideal linearity path.

The graph shows the linear relationship of the pixel position with the linear increment in the measurement value. It takes nearly 160 measurements to reach from pixel 1 to pixel 3, giving a measurement resolution of the test setup as following:

Number of pixels* pixel pitch / number of measurements
=2*45 µm/ 160= 0.5625 µm.

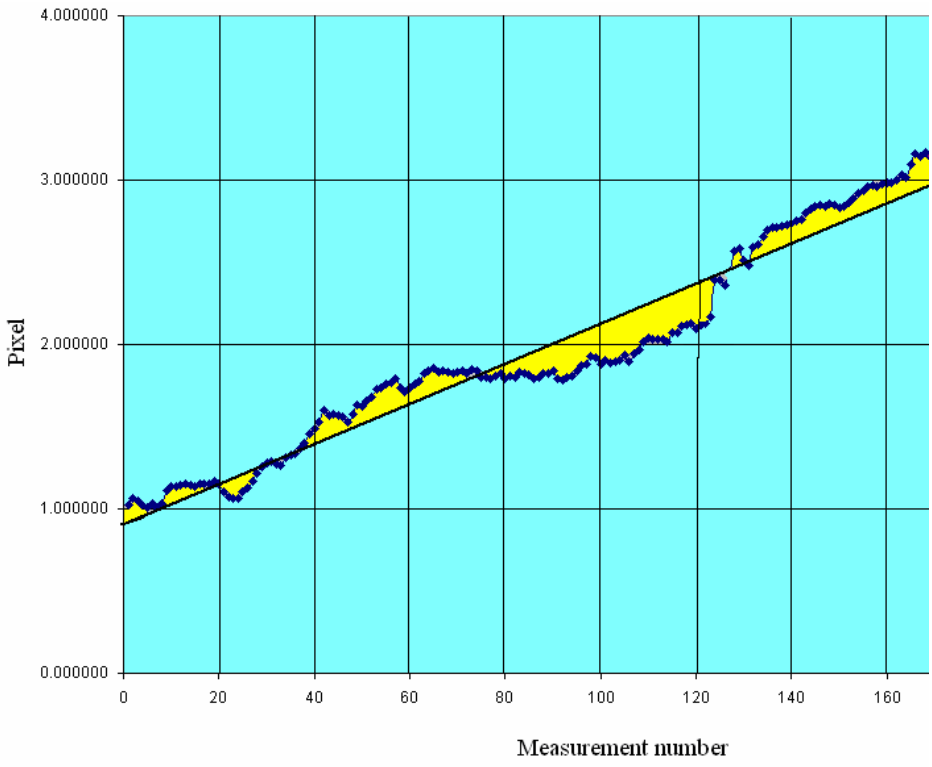

Figure 6.5: *Integral non-linearity: Relationship between successive measurements*

6.4.2 Differential non-linearity (DNL)

The differential non-linearity measures the deviation from the ideal. An ideal converter has the code exactly the same size and a DNL of 0 (zero).

The differential non-linearity curve, as shown in Figure 6.6, gives relationship between the differences in the successive pixel positions, with sub-pixel resolution. The graph shows the relationship among pixel

positions measured on a range of 168 readings. It shows the relative measurement error spread over the ideal value along the x-axis intercepting the y-axis at 0.000000. Barring three measurements out of 168, the error distribution is evenly spread across the ideal value at '0' confirming the sensor functionality.

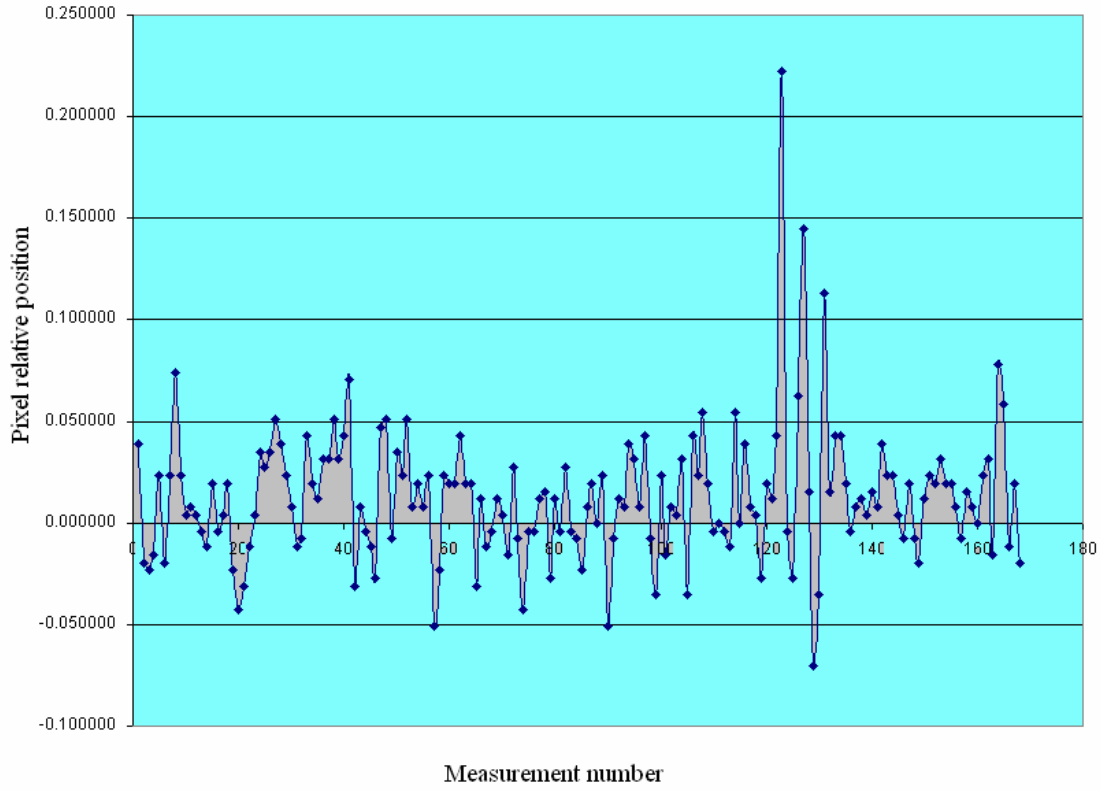

Figure 6.6: *Differential non-linearity: Relationship between successive 'difference' readings*

6.5 The spot shape

Measuring the up and down readings, the spot shape can be determined. When the integration time T_i is varied between its minimum (no pixels crossing the threshold) and maximum (all pixels crossing threshold-photodiode saturation) values, more pixels start crossing the threshold and contribute to the search process. By finding out the pixels crossing the threshold from left and from right during different Ti values, the spot shape can be obtained by plotting the up and down values. This is accomplished by using a predefined configuration file. A sample screen giving the up and down output is shown in figure 6.7.

The waveform shows the exposure of the imager to laser light through LASR integrating the image and image acquisition during the high PHRES signal. When CIN is high, the search for the pixel crossing the threshold in the up and down directions is indicated. It may be noted that that the configuration file stored in the logic analyzer caters to separate up and down computation. COUT high shows the linear sensor output high (*carryout* signal: while computing in forward direction, the output of the linear sensor in reverse direction shows high and vice versa, as the computation is done separately) for the computation in alternate directions, where no pixel is found active and crossing the threshold.

The CKBIN, which is a series of 12 pulses signifying the 12-bit shift register, shown close to QSER (Qserial), gives the serial output. During the first pulse, the data is loaded in the shift register, as explained in the previous chapters, and the serial output is as shown with the LSB part identified by the arrows in the figure.

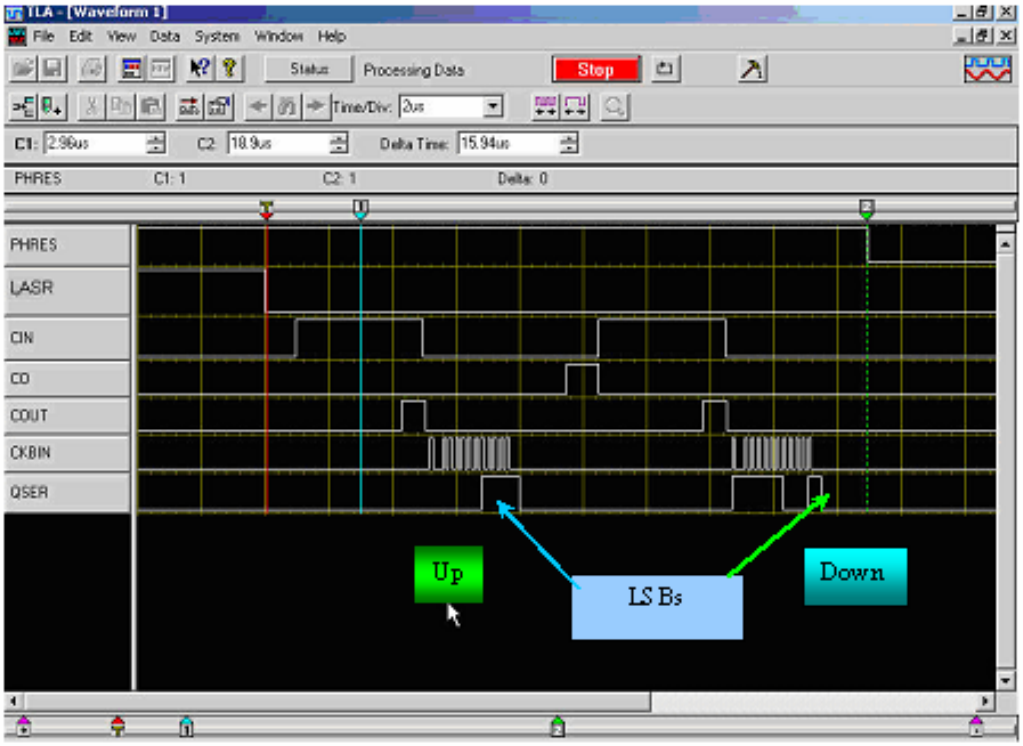

Figure 6.7: *Sample Up/Down waveform*

In the experiment, the minimum integration time is set at 12 ms, as no pixel has crossed the threshold below that value. However, this is subject to intensity of laser spot, ambient light, collimating source, the focusing lens and the optical bench. The readings computed during the forward and reverse directions are plotted, as shown in the Figure 6.8. The setup is adjusted in such a way that the maximum signal is available around the centre pixel, 16.

Despite the non-ideal shape of the reflected light spot, the behaviour of the sensor is predictable and the measurements are within the bounds of the design. However, a better mechanical / optical setup along with higher power laser source would further enhance the effectiveness of the measurements.

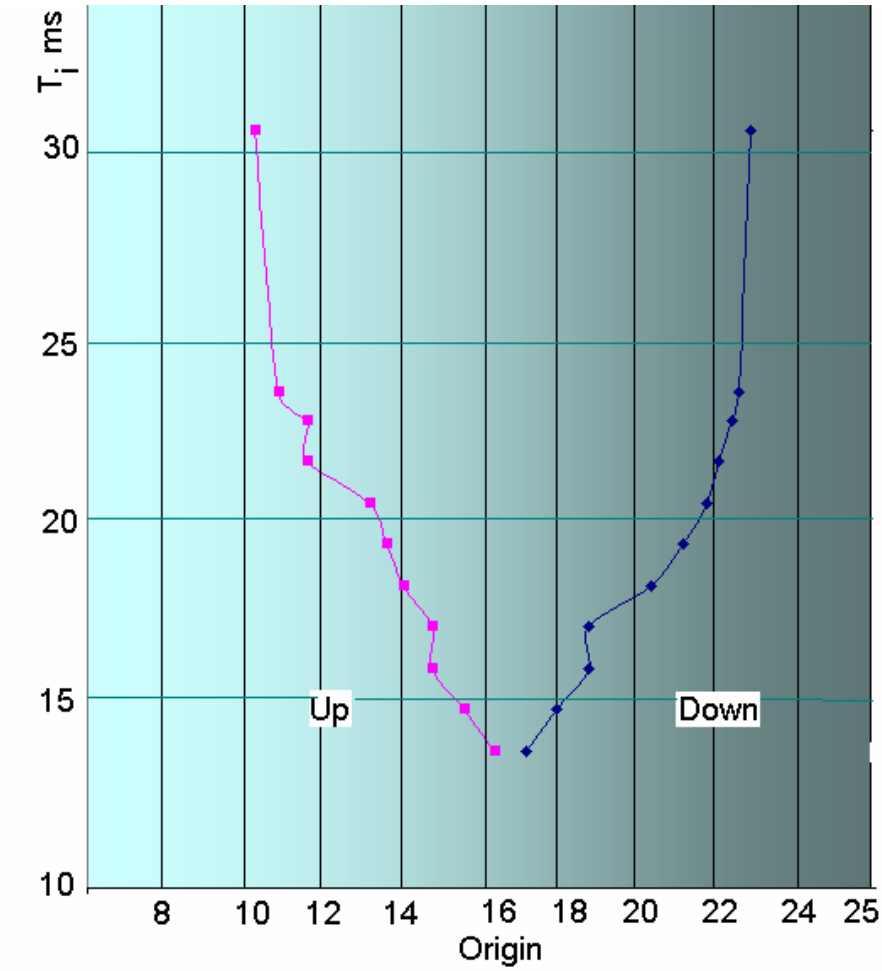

Figure 6.8: *Spot shape*

6.6 Theoretical vs. measured position sensitivity

While log_2 (M+1) bits are required to code (M+1) pixels of the imager, log_2N bits are required to code the sub-pixel fraction, which is obtainable with N measurements. This is formalized [GOT] and experimentally established. Figure 6.10 shows an accuracy of 6% of the pixel pitch with ~ 80 measurements and 3% with ~ 100 measurements, i.e., 50% improvement in the accuracy. However, by increasing the number of thresholds beyond >200 there is just 1% improvement in the accuracy of the measurement.

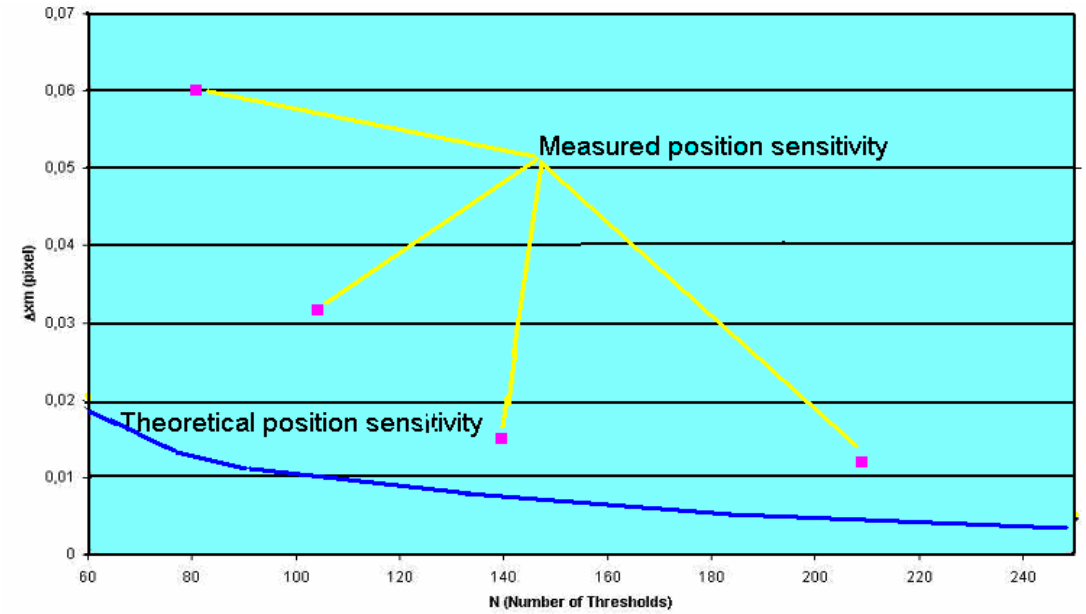

Figure 6.10: *Theoretical vs. measured position sensitivity*

In terms of time versus performance, this is a huge overhead. In real situation, using the multiple thresholding method and N=100 (as described above) distributed along the signal range, a position estimation accuracy of 3% of the pixel pitch has been reported [MAS]. However, this method has been used to measure a single spot position with the sensor working as a position sensitive device. The speed and frame rate are not significant in the design. In this thesis, though the multiple images binarization method is primarily used to measure the position accuracy of a spot, the purpose is to extrapolate the functionality to sheet beam method. Comparing favourably with the above mentioned method, this method has not only achieved the accuracy of 3% of pixel pitch with 128 measurements but also shown potential for high frame rate in the context of 3D measurements. Here, 4 bits are used to code the pixels (since only 4 pixels are considered for measurement) of the array and 8 bits for the sub-pixel resolution for 128 measurements.

6.7 Post-testing simulation

Since the device has shown the performance as per the design, efforts are on to improve the design. As a first step, the practical timing value of 125ns (8MHz), as per the Figure 6.11, is to be emulated in the simulation process. This is to estimate the data rate after extrapolation to higher pixel count in the array.

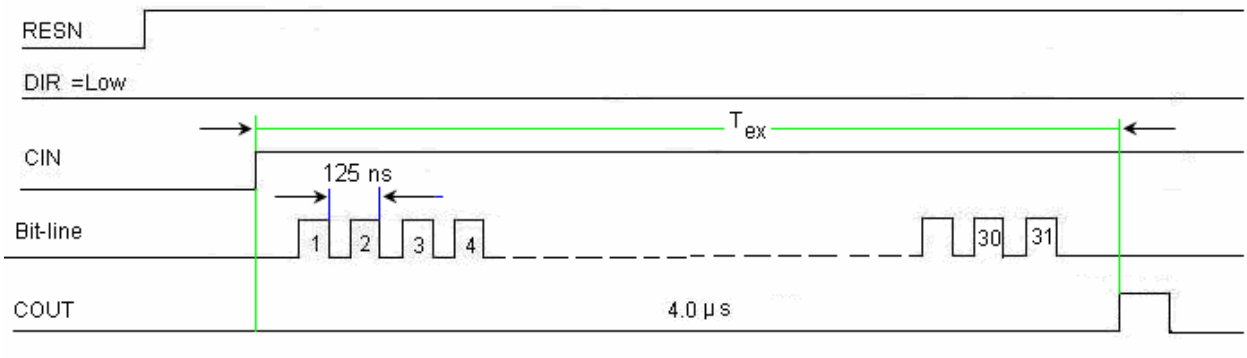

Figure 6.11: *Measured frequency on the bit-line of the chip*

Before continuing with the post testing simulation process, it is to be noted that four weak inverters are used in the design (two in the pixel and two in the feedback process between the bit-lines, BLF and BLB), in order to avoid the conflict in timing process of pulse generation on carryout and on bit-line. The slow inverters are custom built with L /W values: PMOS 1.5 µm / 4 µm; NMOS: 0.6 µm / 4 µm respectively. Since the standard minimum size inverters (Cadence library) perform within the design constraints, linear arrays of 31, 100 and 2D arrays of 31 x 31 and 100 x 100 pixels are simulated with the extracted layout and the performance is compared, as per Table 6.1. This shows that the linear device pulse speed can be enhanced >8 times with the new design at no extra efforts and penalty.

The single operating cycle time is calculated with the following formula:

$$OCT = ((1/PF) \times (M+1) \times 2) \quad (6.1)$$

Where PF is the pulse frequency, 2 x (M+1) is the number of pixels (in forward and reverse directions).

The frame rate, FR, is calculated with the following formula:

$$FR = OCT \times N_t \text{ fps} \quad (6.2)$$

where N_t is the number of image threshold operations.

The range map rate is calculated with the following formula:

$$RR = FR / (M+1) \text{ range maps/s} \quad (6.3)$$

The 2D array of 31 x 31 pixels with minimum size standard inverters gives a frame rate of 8.4 K fps and a range map rate of 271-range maps/s and when extrapolated to an array of 100 x 100 pixels gives a frame rate of 1.35 K and 13.5-range maps/s.

Table 6.1: *frequency values obtained in the simulation with slow and standard inverters during design improvement*

Device	**PF MHz**	**OCT= ((1/PF) x (M+1) x 2) µs**	**FR = OCTx N_t fps (N_t=128)**	**RR= FR/(M+1) rps**
31 pixel array (Real)	8	7.8	1 K	-
31 pixels with minimum size standard inverters (extracted & simulated)	66.7	0.93	8.4 K	-
31 x 31 pixel array With standard inverters (extrapolated)	66.7	0.93	8.4 K	**271**
100 pixels with standard inverters (extracted & simulated)	34.5	5.8	1.35 K	-
100 x 100 pixel array (extrapolated)	34.5	5.8	1.35 K	**13.5**

6.8 Related work

The discussion so far has been on the design and testing of the CMOS imager for active triangulation based sheet beam method, with a brief overview of the state of the art in 3D measurement sensors.

In this section, a comparison of the more closely related developments in CMOS imagers is presented. Though the device presented here is a linear sensor of 31 pixels finding the position of a light spot, the architecture is for a 2D sensor using sheet beam approach for 3D measurement. Hence, by extrapolating on scaling and projecting to larger pixel array, a fair comparison with the state- of- the- art developments CMOS imagers for 3D measurements is possible.

There are several factors to be considered in the comparison of the result: the technology used, the pixel size, the array size, the algorithm implemented for obtaining accuracy, speed and resolution.

The device presented in its form cannot be compared for the performance with other devices in this category. Since, this work is mainly to investigate on the feasibility of the approach, optimization of the design is not considered. However, by taking the post- testing simulations in to account, better results can be achieved with the same design, which makes the comparison fair. Though several CMOS smart imager designs exist in the literature for 3D measurement, only a few are mentioned here because of the common features with the reported work, with respect to the algorithm, implementation, approach etc. However, the devices discussed here are the most cited in literature for the sheet beam based 3D measurements using active triangulation method. The next section illustrates the salient features of various devices of the state of the art and proposes a comparison. However, this is not exhaustive, as explained previously.

6.8.1 Comparison of state-of-the-art 3D imagers (Reference: Chapter 2, section 2.6)

Table 6.2: *Comparison with different state of the art CMOS smart sensors*

Chip	CMOS process	Number of pixels	Pixel size µm x µm	Sub-pixel resolution	accu-racy %	fps	Range maps/s
1	2.0 µm	28x32	28x28	-	0.5	1K	1K
2	2.0 µm	64x64	62 x 62	-	-	100	100
3	0.35 µm	128x128	19.5x 19.5	0.06 pixel 1.2 µm	0.4	10K	12/600
4	0.35µm	192x124	46.4x 54	500 µm	-	24K	60
5	0.35µm	320x240	11.2x 28	0.7 pixel		3.3 K	15
6	0.6 µm	640x480	12x12	0.2 pixel			65.1
7	0.35µm	128x128	19.5x 19.5			233K	1052
8				Sub mm		2K	500
9	0.35µm	31x31	45 x40	0.06 pixel	0.064	8.4 K	271

Table 6.3: *References used in the discussion on related work*

Chip ref.	Details
1	A very fast VLSI rangefinder *Kanade, T.; Gruss, A.; Carley, L.R.;* Robotics and Automation, 1991. Proceedings., 1991 IEEE International Conference on , 9-11 April 1991 Pages:1322 - 1329 vol.2
2	V. Brajovic, K. Mori and N. Jankovic. 2001. 100 frames/s CMOS Range Image Sensor,. *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 256 . 257.
3	T Nezuka, M. Ikeda and K. Asada. 2002. .A Smart Position Sensor With Row Parallel Position Detection for High Speed 3-D Measurement,. *in Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 101 . 104.
4	S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda. 2001. .A 48k frame/s CMOS Image Sensor for Real-time 3-D Sensing and Motion Detection,. *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 94 . 95.
5	T. Sugiyama, S. Yoshimura, R. Suzuki and H. Sumi. 2002. .A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory,. *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 434 . 435.
6	Y. Oike, M. Ikeda and K. Asada. 2003. .640 x 480 Real-Time Range Finder Using High-Speed Readout Scheme and Column-Parallel Position Detector,. *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 153 . 156.
7	Yusuke Oike, M. Ikeda and K. Asada.2004 : A 375 x 365 3D 1k frame/s Range-Finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy *IEEE Int. Solid-State Circuits Conf. (ISSCC)*..
8	Vladimir Brajovic : Proceedings of the 2004 IEEE international Conference on Robotics & Automation, New Orleans. LA. April 2004:Fast Row-Parallel CMOS Range Image Sensor
9	The sensor presented in this thesis

Table 6.2 gives the comparative chart of the state of the art 3D imagers for range measurement, and the related references / sources are presented in Table 6.3.

It may be noted that the Table 6.2 is not exhaustive in comparison but is accurate to the best of understanding of the publication, but still some inaccuracies might be inadvertently present. Specifications for a few devices are not complete since the related publications explicitly do not mention them. Comparisons are also subject to different technologies, different specifications.

Chapter 7

Conclusions

This chapter summarizes the 3D measurement problem dealt with in the thesis, suggests a smart CMOS image sensor to address the active triangulation methods, and presents its main innovative features. It also outlines future work on the CMOS imagers for 3D measurement and gives sample application scenarios of the proposed scheme.

7.1 Overview

Real-time 3D imaging applications generate massive amounts of data: be it for tracking, estimating position, or reconstructing object profile. Hence, they demand high speed, highly accurate and high frame rate imagers to be able to function in real time. This thesis addresses the real time 3D measurement problems, particularly the active triangulation based sheet beam projection (one of the most commonly used methods for acquiring range data) and suggests imager architecture, in CMOS, for real time, high speed and highly accurate data processing.

7.2 CMOS imager with a new 2D architecture

The smart CMOS imager implements a novel image processing technique at pixel level using an asynchronous position-to-pulse conversion mechanism, which is able to extract the position of the impinging light spot during image acquisition with high image estimation accuracy. Inherent in the design is a high level of parallelism to achieve massive parallel processing at high frame rate, required in 3D computation problems.

7.2.1 Reduction in image processing complexity

F**o**llowing the proposed approach, the vision sensor will be organized as an ensemble of linear sensor arrays working in parallel and processing the entire image in slices. Each linear image sensor works as a Position Sensitive Device (PSD), finding the centroid of the portion of the light impinging on it, thus reducing the complexity of the image-processing task, from O (N^2) to O (N).

7.2.2 Multiple images binarization instead of multiple thresholding- time as parameter instead of voltage

A multiple images binarization technique, where image processing is carried out during image acquisition, is investigated to obtain high sub-pixel resolution at high frame rate. This is realized by presetting the threshold value and binarizing the image several times, while the image is being integrated.

While achieving sub-pixel resolution, this approach also optimizes the image processing cycle time since, both image acquisition and image processing can be carried out simultaneously, once the pixels cross the preset threshold voltage during the image integration time. This approach achieves a comparable result of sub-pixel resolution with the standard multiple thresholding technique and does not require additional and analog hardware to generate threshold ramp. In other words, by adopting the multiple images binarization

method, one can avoid the complexity of additional hardware, minimize the image processing time and still achieve better sub-pixel resolution.

Experimental results of a prototype of a 31 pixels linear sensor array demonstrate the adopted approach is suitable for the 3D measurement task due to its high speed (projected value 271 range maps/sec) and high accuracy (0.6 pixel) which are the two main figures of merit for this kind of problem. The results are comparable to the state of the art solutions.

7.3 Advantages of the approach

Since the linear sensor design is modular, extending the design to larger array size is relatively easy. For example, if the pixels in the array and the number of stages in the counter are to be increased, it just amounts to reusing the custom blocks designed in Cadence.

Since the sensor architecture is parallel, extending the design to two dimensions is possible just by replicating and closely placing the linear sensors as a 2D structure.

By adapting pixel level processing and using non conventional A/D conversion close to the input analog photo signal for binarising the image, high frame rate is achieved in addition to keeping the hardware complexity within implementable bounds.

Using the multiple images binarization method, image processing time is significantly reduced, thus improving the frame rate and resolution. In addition, hardware overhead associated with the multiple thresholding method (used to achieve higher resolution), is avoided.

The proposed architecture is scalable since the design considers a balanced analog and digital mixed implementation. The photo signal is converted into binary just after the comparator stage: at the earliest in the image processing cycle. Since the majority of the pixel, and hence the array, are digital, scalability in the design is achievable. As the photo diode uses a large area, it can also be scaled without loss of performance, when the rest of the circuit is scaled.

The pulse-stream architecture is fully asynchronous, generating a digital burst with a frequency depending on the propagation delay between neighbouring pixels. This architecture requires only an input signal as a trigger for starting the signal processing of all the N linear sensors. No clock is required for pixel selection within the sensor array. This makes the proposed architecture tolerant to delay of each element.

The asynchronous approach allows the sensor architecture to be modular because the pulse generation process onto the bit-line, as well as the propagation delay between two neighbouring pixels, are self-adapting with respect to the imager dimensions. This can be obtained by using the feedback network as an acknowledge signal for the digital pulse sent onto the bit-line.

The proposed architecture still achieves good performance of 4 bit accuracy without compensating for the critical parameters, viz., transistor mismatch, parasitic capacitance, thermal, flicker or shot noises and temperature variation which typically affect a device performance. This is an important property in the context of design re-use and technology migration.

While the position estimation process is still linearly related to the size of the array with its number of pixels, the proposed solution offers the advantage of a single type of pixel, suitable for all imager dimensions without technology constraints, temperature variations or other parameter variations.

The salient features of this work are the position to pulse stream conversion, asynchronous design, high parallelism and modular architecture resulting in high sub-pixel resolution.

7.4 Future work

Improving the speed of the position estimation process and optimizing the architecture are the two important issues. The speed is mainly limited by the type of the search mechanism used, typically for one thresholding process.

Though implementing programmable windowing feature to identify the approximate winning pixel position at first and working on the RoI (Region of Interest) will speed up the search process. However, this may involve major changes in the architecture. Hence, immediate task will be to speed up the operation by incorporating more efficient search mechanism in the existing row parallel linear architecture, as described below, which can double the process speed.

The method adapted in the position to pulse conversion, used in this thesis, is to commence the search operation for finding a pixel crossing the threshold (0 to 1 transition) in the forward direction and continue until the T_{exm} is exhausted and start the search in the reverse direction. Hence, The total time spent for one cycle of operation is $2(M+1)\,\tau$, where M+1 is the total number of pixels in the array and τ is

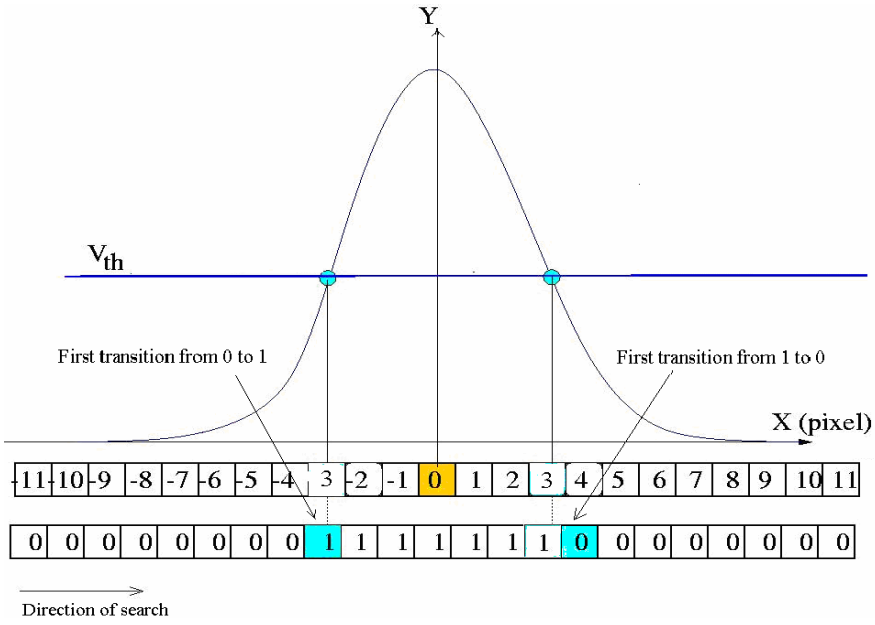

Figure 7.1: *Unidirectional search replacing bi-directional search mechan*ism

the propagation time. Since, it is not economical to interrogate each pixel in a large array to find the winning pixel; an efficient search is to be implemented.

Instead of the above-mentioned approach, if the search operation is continued in the same direction, as shown in Figure 7.1, after finding the first transition (0 → 1), for the opposite transition (1 → 0), by averaging the two positions, one can obtain the centroid. This would result in $T_{exm} = (M+1)\,\tau$, which is half of that mentioned in the previous approach. This is the worst-case cycle time. Hence, without major changes in the architecture one can immediately double the process time. By stopping the execution when the right transition is found would further speed up the process.

The reduction in the pixel dimension, probably by sacrificing some fill-factor, resizing the photodiode area, and simplifying the pixel electronics would improve the performance of the device. The most expensive block in terms of device real estate is the clocked comparator with 14 transistors. The binarization can be optimized by replacing this circuit with a simpler clocked comparator, made of just eight transistors, which also has no dc power consumption. This design is being implemented.

The device tested is a linear sensor only, as the principle is to be proved in one dimension and then extend it to the 2D architecture. The actual 3D measurement issue can be addressed only with a 2D architecture using the sheet beam approach. The sensor design is not optimized in terms of size and functionality.

Carry propagation time is dependent on the pixel pitch. In the present architecture, irrespective of a pixel reaching the threshold, the cycle time T_{exm} is constant. Hence, if there are more pixels in the array, the propagation delay will proportionately increase. A mechanism to stop the computation and reverse the direction of the search, immediately after a pixel crossing the threshold, would increase the speed of computation.

Bibliography

[ALE] J. W. Alexander, S. Lee, C.-C. Chen, "Pointing and Tracking concepts for deep-space missions," in Free-Space Laser Communication Technologies XI, Proc. of SPIE vol. 3615, pp. 230-249, 1999.

[AND] Andreou A., Boahen K., Pouliquen P., Pavasovic A., Jenkins R., and Strohbehn K, "Current-Mode Subthreshold MOS Circuit for Analog Neural Systems," *IEEE Transactions on Neural Networks*, Vol. 2, No. 2, pp. 205-213, 1991.

[BLA] Francois Blais, "Review of 20 years of range sensor development", Journal of Electronic Imaging 13(1), 231– 240 (January 2004).

[BOH] Boahen, K.A, "A retinomorphic vision system", Micro, IEEE, Volume: 16 , Issue: 5 , Pages:30 – 39, Oct. 1996.

[CUL] Culurciello, E.; Andreou, A.G., " A comparative study of access topologies for chip-level address-event communication channels Neural Networks", IEEE Transactions on ,Volume: 14 , Issue: 5 , Sept. Pages:1266 – 1277, 2003

[BAK] M. de Bakker, P. W. Verbeek, E. Nieuwkoop and G. K. Steenvoorden, "A Smart Range Image Sensor", *in Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 208-211, 1998

[BAR] R. Baribeau, and M. Rioux, "Influence of Speckle on Laser Range Finders," Appl. Opt., 30, 2873—2878, (1991).

[BER1] Berthold Klaus Paul Horn, "Robot vision", MIT press, Cambridge & McGraw-Hill, Newyork, 1986

[BER2] Beraldin, J.A. Blais, F., Cornouyer, L., Rioux, M., El-Hakim. S, " 3D imaging for rapid response on remote sites", SIGGRAPH'99 Technical Sketches, pp. 225, Los Angeles, August 8-13, 1999.

[BER3] J.-A. Beraldin, F. Blais, L. Cournoyer, G. Godin, and M. Rioux, " *Active 3D Sensing",* published in Modelli E Metodi per lo studio e la conservazione dell'architettura storica, University: Scuola Normale Superiore, Pisa, 10: 22-46;2000. NRC 44159. April 2000.

[BER4] J.-A. Beraldin, F. Blais, M. Rioux, L. Cournoyer, D. Laurin, and S.G. MacLean, "Eye-safe digital 3D sensing for space applications," Opt. Eng. 39(1): 196-211; (2000).

[BES] P. Besl, "Advances in Machine Vision", Springer-Verlag, chapter 1 - Active optical range imaging sensors, pp. 1–63, 1989.

[BLA] Blais, F, "Review of 20 Years of Range Sensor Development", Journal of Electronic Imaging, 13(1): 231-240. January 2004.

[BRA1] V. Brajovic and T. Kanade, "Computational sensor for visual tracking with attention", IEEE Journal of Solid-State Circuits, vol. 33, no. 8, pp. 1199 – 1207, Aug.1998.

[BRA2] V. Brajovic, K. Mori and N. Jankovic, "100 frames/s CMOS Range Image Sensor", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 256 . 257, 2001.

[BRA3] Vladimir Brajovic´ and Takeo Kanade, " When are smart sensors smart? An example of an illumination-adaptive image sensor", Sensor Review, Volume 24 · Number 2 pp. 156–166, Emerald Group Publishing Limited, 2004 .

[CHA] David Chapman, Sabry El-Hakim, "Short-baseline active triangulation for cad reconstruction of room sized industrial environments", IAPRS, Vol. XXXIII, Amsterdam, Vol 5A, pp 122-129, 2000.

[CHE] T. Chen, P. Catrysse, A. E. Gamal and B. Wandell, "How Small Should Pixel Size Be?", *in Proc. of SPIE*, vol. 3965, pp. 451-459, 2000.

[DAV] James Davis, Diego Nehab, Ravi Ramamoothi, Szymon Rusinkiewicz. "Spacetime Stereo: A Unifying Framework for Depth from Triangulation," IEEE Trans. On Pattern Analysis and Machine Intelligence (PAMI), vol. 27, no. 2, Feb 2005.

[DEL] T. Delbrück, *Investigations of Visual Transduction and Motion Processing*, Ph. D. Thesis, California Institute of Technology, 1993.

[DIC1] A. Dickinson, B. Ackland, E. Eid, D. Inglis, and E. Fossum, "A 256×256 Active Pixel Image Sensor with Motion Detection," in *ISSCC95 Techincal Digest*, February 1995.

[DIC2] A. Dickinson, S. Mendis, D. Inglis, K. Azadet, and E. Fossum, "CMOS Digital Camera With Parallel Analog-to-Digital Conversion Architecture," in *1995 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors*, April 1995.

[DEC] S. Decker, R.McGrath, K. Brehmer, and C. Sodini, "A 256x256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output," in *ISSCC Digest of Technical Papers*, pp. 176–177, (San Fransisco, CA), February 1998.

[DEW]. S. Deweerth, "Analog VLSI circuits for stimulus localization and centroid computation," International Journal of Computer Vision, vol. 8 (2), pp. 191-202,1992.

[DUM] Martin Dumberger, "Taking the Pain out of Laser Triangulation", Sensor technology and design, July 2002.

[ELE] Elisenda Roca, Servando Espejo, Rafael Domínguez-Castro and Angel Rodríguez-Vázquez, "Light-Sensitive Devices in CMOS", internet source , gratefully acknowledged.

www.imse.cnm.es/Proyectos/dictam/2ND_PHASE/Dissemination/FULL_TEXT/CMOS/

[EVA] M. W. Evans, "Minimal Logic Synchronous Up/Down Counter Implementation for CMOS," U.S. Patent no. 4,611,337, Sept. 1986.

[FOS] Eric R. Fossum, "CMOS Image sensors: Electronic camera-on-a-chip", IEEE Transactions on Electron Devices. Vol.44, No.10, pp.1689-98, Oct.1997.

[CUM] R. Etienne-Cummings, "Intelligent Robot Vision Sensors in VLSI", Autonomous Robots, Vol. 7, No. 3 pp.225-237, 1999.

[GAM] Abbas El Gammal, David Yang and Boyd Fowler, "Pixel Level Processing – Why, What and how?" SPIE, Vol. 3650, pp.2 - 13, 1999.

[GOT] Massimo Gottardi, “Novel position detection algorithm for VLSI implementation”, ITC-irst technical report.

[GRU] Andrew Gruss, Shigeyuki Tada and Takeo Kanade, “ A VLSI smart sensor for fast range imaging”, Proceedings of the 1992 IEEE/RSJ International Conference of Intelligent Robots and Systems, Raleigh, NC., July 7-10,1992.

[HAS] R.R. Harrison and C. Koch, “A robust analog VLSI sensor based on the visual motion system of the fly”, Autonomous Robots, vol.7, pp.211-224,1999.

[HAK] El-Hakim, S.F., Beraldin, J. A,” On the integration of range and intensity data to improve vision-based three dimensional measurements”, SPIE Proc., Vol. 2350, Videometrics III, pp. 306-321 1994.

[JAR] Jarvis, R, “A perspective on range-finding techniques for computer vision”, IEEE Trans. Pattern Analysis Mach. Intell. **5**: 122–139, 1983.

[KOC] Christof Koch and Bimal Mathur, “ Neuromorphic vision chips”, IEEE Spectrum, pp 38-46, May 1996.

[LAV] Joseph P. Lavelle, Stefan R. Schuet, Daniel J. Schuet, “High speed 3D scanners for real time 3D processing”, SIcon/04-Sensors for Industry conference, New Orleans, Louisiana, USA, 27-29 January, 2004.

[LAN] R. Lange and P. Seitz .Solid-State Time-of-Flight Range Camera,. *IEEE Journal of Quantum Electronics*, vol. 37, no. 3, pp. 390-397, 2001.

Lazzaro, J, “ Low-power silicon spiking neurons and axons”, Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on ,Volume: 5 , 3-6, Pages:2220 - 2223 vol.5, May 1992.

[LIU] Shih-Chii Liu; Douglas, R, “Temporal coding in a silicon network of integrate-and-fire neurons”, IEEE Transactions on Neural Networks ,Volume: 15 , Issue: 5 , Pages:1305 – 1314, Sept. 2004.

[KOC] C. Koch and B. Mathur, “Neuromorphic vision chips”, IEEE spectrum, vol.33, no, pp 38-46, May 1996.

[KRY] A. Krymski, D. Van Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, “A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor”, *IEEE Symp. VLSI Circuits Dig. of Tech. Papers*, pp. 137 – 138, 1999.

[KLE] S. Kleinfelder, S. Lim, X. Liu and A. E. Gamal, “A 10k frame/s 0.18 µm CMOS Digital Pixel Sensor with Pixel-Level Memory”, *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 88 - 89, 2001.

[MAL] Elias N. Malamas, Euripides G.M. Petrakis, Michalis Zervakis, Laurant Pettit and Jean-Didier Legat, "Industrial Vision: Systems, Tools and Techniques", Image and Vision Computing, Vol. 21, No. 2, pp. 171-188, February 2003,.

[MAN] J. Mann, “Implementing Early Visual Processing in Analog VLSI: Light Adaptation”. *Proc. of SPIE-Visual Information Processing: from Neurons to Chips*, Vol. 1473, pp. 128-132, 1991.

[MAR] Neil Martson, “ Solid state inaging: a critique of thr CMOS sensor”, Ph.D thesis, Univ. of Edinburgh, November, 1998.

[MAS] Nicola Massari, Lorenzo Gonzo, Massimo Gottardi, and Andrea Simoni, "A fast CMOS optical position sensor with high sub-pixel resolution", IEEE Transactions on Instrumentation and Measurement, VOL. 53, NO. 1, February 2004.

[MAS] Nicola Massari, Lorenzo Gonzo, Massimo Gottardi, and Andrea Simoni, "High speed Digital CMOS 2D Op A fast CMOS optical position sensor with high sub-pixel resolution", IEEE Transactions on Instrumentation and Measurement, VOL. 53, NO. 1, February 2004.

[MAY] A. Mäkynen and J. Kostamovaara, "Linear and sensi-tive CMOS position-sensitive photodetector," Electronics letters, Vol. 34 (12), pp.1255-1256, (1998).

[MEM] Spartan –IIE Development board user's guide, Memec Design Services, Version 1.0, November, 2001.

[MEN] S. Mendis, S. Kemeny, R. Gee, B. Pain, C. Staller, Q. im, and E. Fossum, "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," *IEEE Journal of Solid State Circuits* **32**, pp. 187–197, February 1997.

[MOI] Alireza Moini, "Vision chips or seeing silicon", Technical Report, Centre for High Performance Integrated Technologies and Systems, The University of Adelaide, March 1997.

[MUL] R.S. Muller and T.I. Kamins, *Device Electronics for Integrated Circuits-2nd edition*, John Wiley & Sons, 1986.

[MUN] Mundy, J. & Porter, G. *Three-dimensional machine vision*, Kluver Academic Publishers, chapter 1 - A three-dimensional sensor based on structured light, pp. 3–61, 1987.

[NAY] Nayar, S., Watanabe, M. & Noguchi, M. Real-time focus range sensor, *Proceedings of IEEE International Conference on Computer Vision*, pp. 995–1001, 1995.

[NEZ1] T. Nezuka, M. Hoshino, M. Ikeda and K. Asada "A Position Detection Sensor for 3-D Measurement", *in Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 412- 415, 2000.

[NEZ2] T Nezuka, M. Ikeda and K. Asada, "A Smart Position Sensor With Row Parallel Position Detection for High Speed 3-D Measurement", *in Proc. of European Solid-State Circuits Conference (ESSCIRC)*, pp. 101- 104, 2002.

[OIK1] Yusuke Oike, Makoto Ikeda and Kunihiro Asada," Smart access image sensors for high-speed and high-resolution 3D measurement based on light-section method", *Intelligent Automation and Soft Computing*, Vol. 10, No. 2, pp. 105-128, 2004.

[OIK2] Y. Oike, M. Ikeda and K. Asada., " A 375 x 365 3D 1k frame/s Range-Finding Image Sensor with 394.5 kHz Access Rate and 0.2 Sub-Pixel Accuracy", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers* 2004.

[PAI] F. Paillet ASIC/SOC'2000, " Design solutions and techniques for vision system on a chip and fine grain parallelism circuit integration", Washington DC, USA, September 16, 2000.

[PAS] Walt Pastorius, "Triangulation sensors: An overview", white paper, www.lmitechnologies.com, Oct.2001.

[PIE] P.J. Pietraski, Z. Zojceski, D.P. Siddons, G.C. Smith and B. Yu, "Digital Centroid-Finding Electronics for High-Rate Detectors", IEEE Transactions On Nuclear Science, Vol. 46, No. 4, August 1999.

[POU] Denis Poussart and Denis Laurendeau, "Chapter 3: 3D Sensing for Industrial Computer Vision", in *Advances in Machine Vision (Volume Applications and Architectures)*, pp. 122-159, Springer Verlag, 1989.

[RIO] Rioux, M, " Laser range finder based on synchronized scanners", *Applied Optic*s, **2**3, 3837-384, 1984.

[SCH1] R. Schwarte, "Principles of 3-D Imaging Techniques", in Handbook of Computer Vision and Applications, B. Jähne, H. Haussecker and P.Geissler (Eds.), Academic Press, (1999).

[SCH2] Christie Schrodenger (Ed.), "Guidance, Naviagation, and Control", Aerobraking and Impact Attenuation Subsystems, NASA & University of Texas at Austin Space Consortium, December 1994.

[SIM] Andrea Simoni, Lorenzo Gonzo and Massimo Gottardi, "Integrated Optical Sensors for 3-D Vision", Sensors, 2002. Proceedings of IEEE, Vol. 1, 12-14, June 2002.

[SLE] Slevogt, H. *Technische Optik*, pp. 55–57, 1974.

[STA] Mircea R. Stan, Alexandre F. Tenca and Milos D. Ercegovac, "Long and Fast Up/Down Counters", IEEE Transactions on Computers, Vol.47, No. 7, July 1998.

[STO] D. Stoppa, "Integrated CMOS optical sensors for advanced applications", Univ. of Trento. Ph.D. Thesis, No 2002/01, 2002.

[STR] T. Strand, "Optical three dimensional sensing", *Optical Engineering*, 24(1):33–40, Jan-Feb 1983.

[SUN] Chao Sun, Guang Yang, Christopher Wrigley, Orly Yadid-Pecht; and Bedabrata Pain*, "*A Smart CMOS Imager with On-chip High-speed Windowed Centroiding Capability", R9-1, Jet Propulsion Laboratory, California Institute of Technology, under contract with NASA.

[SUG] T. Sugiyama, S. Yoshimura, R. Suzuki and H. Sumi, "A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 434 - 435, 2002.

[SZ1] S. Sze, "Physics of semiconductor devices", 2nd edition, *John Wiley &Sons*, (1981).

[SZ2] S. Sze, "Semiconductor Devices, Physics and Technology", 1st edition, *John Wiley & Sons*, (1985).

[ULL] A. Ullrich, N. Studnicka, and J. Riegl, "Long-Range High-Performance Time-of-Flight-Based 3D Imaging Sensors". *in Proc. of IEEE Int. Symp. 3D Data Processing Visualization and Transmission*, pp. 852- 856, 2002.

[VAN] Vanam Upendranath, Massimo Gottardi, Alessandro Zorat, " Smart CMOS image sensor for 3D measurement", 6th conference on Optical 3D Measurement techniques, , ETH, Zurich, Switzerland, September, 22 -23, 2003.

[VIA] L. Viarani, D. Stoppa, L. Gonzo, M. Gottardi, and A. Simoni, " A CMOS Smart Pixel for Active 3-D Vision Applications", *IEEE Sensors Journal,* vol. 4, no. 1, pp. 145-152, 2004.

[VIT] Vittoz, E.A., "Analog VLSI for collective computation", Electronics, Circuits and Systems, 1998 IEEE International Conference on ,Volume: 2 , 7-10 Pages:3 - 6 vol.2, Sept. 1998.

[YAD1] O. Yadid-Pecht, R. Ginosar, and Y. Diamand, "A random Access Photodiode Array for Intelligent Image Capture," *IEEE Transactions on Electron Devices* **38**, pp. 1772–1780, August 1991.

[YAD2] O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E. Fossum, "CMOS Active Pixel Sensor Star Tracker with Regional Electronic Shutter," *IEEE Journal of Solid State Circuits* **32**, pp. 285–288, February, 1997.

[YAM] Atsushi Yamashita, Toru Kaneko, Shinya Matsushita, Kenjiro T. Miura and Suekichi Isogai: "Camera Calibration and 3-D Measurement with an Active Stereo Vision System for Handling Moving Objects", Journal of Robotics and Mechatronics, Vol.15, No.3, pp.304-313, June 2003.

[YOS] S. Yoshimura, T. Sugiyama, K. Yonemoto and K. Ueda, "A 48k frame/s CMOS Image Sensor for Real-time 3-D Sensing and Motion Detection", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. of Tech. Papers*, pp. 94 – 95, 2001.

[WAN] Y.T. Wang and B. Razavi, "An 8-Bit 150-MHz CMOS A/D Converter," IEEE J. Solid-State Circuits, Vol. SC-35, pp. 308-317, March 2000.

[WAT] David A. Watola and Jack L. Meador, "Competitive learning in Asynchronous-pulse-density-integrated circuits", in Analog VLSI Neural Networks, Yoshiyasu Takefuji (Ed.), Kluwer Academic Publishers, 1992.

[WEC] G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integrating mode," *IEEE Journal of Solid-State Circuits*, vol. 2, pp. 65–73, September 1967.

[WHI] M. H. White *et al.*, "Characterization of surface channel CCD image arrays at low light levels," *IEEE Journal of Solid-State Circuits*, Vol. 9, no. 1, pp. 1–13, 1974.

[ZUF] J.C. Zufferey et al., "Vision-based Navigation from Wheels to Wings", Autonomous Systems Lab, EPFL Zurich, http://asl.epfl.ch/aslInternalWeb/ASL/publications/uploadedFiles/ Zufferey_Beyeler_Floreano_IROS03.pdf

Appendix A

A.1: Terminology related to the measurements and analysis of data

The terms describing the performance of sensors are defined according to the IEEE Standard Dictionary of Electrical and Electronics Terms (IEEE 1996):

Accuracy is the degree of correctness with which a measured value agrees with the true value.

Random error is a component of error whose magnitude and direction vary in a random manner in a sequence of measurements made under nominally identical conditions.

Systematic error is the inherent bias of a measurement process or of one of its components.

Differential non-linearity is the percentage departure of the slope of the plot of output versus input from the slope of a reference line.

Integral non-linearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the centre of the quantization band.

Precision is the quality of coherence or repeatability of measurement data, customarily expressed in terms of the standard deviation of an extended set of measurement results.

Resolution describes the degree to which closely spaced objects in an image can be distinguished from one another.

Incremental sensitivity is a measure of the smallest change in stimulus that produces a statistically significant change in response.

A.2: Terminology related to the triangulation and measuring geometry [PAS]

At the surface, the laser projects a spot of light at position A. At an angle to the laser beam, a lens is used to form an image or "picture" of this spot at an image plane at position A1. If the surface is farther away from the sensor, the spot on the surface is formed at position B, and the location of the spot shifts to position B1. By determining the position of the imaged spot and calculating the angles involved, the distance from the sensor to the surface can be determined.

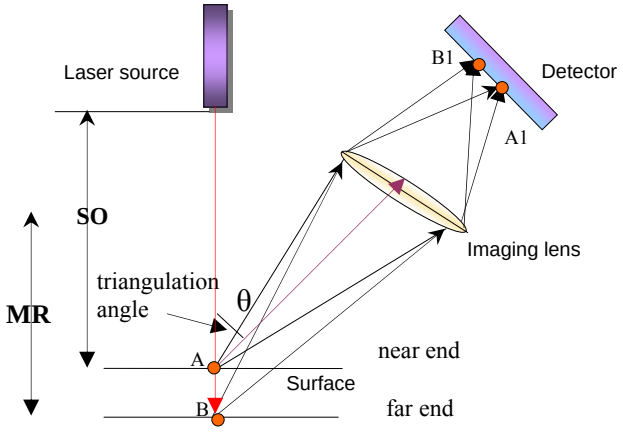

Figure A.1: *Triangulation principle and measuring geometry terms*

The triangulation angle is a major factor in sensor performance determination. In general, as the triangulation angle increases, for a given optical magnification and detector geometry, the sensor range decreases and resolution increases. Practically, the laser triangulation angle may be as low as 10 degrees for a low-resolution sensor and up to about 45 degrees for a high-resolution sensor. The resolution of triangulation sensors improves with smaller measuring range, but this does not necessarily improve the quality or accuracy of measurement.

Stand Off Distance, SO is the distance from the sensor to the middle of the MR. At the SO is normally where characteristics of the sensor are optimised.

Sensors are available in a variety of stand off values to suit most applications. As a rule, sensors with higher accuracy will have shorter stand off, to keep the sensor package size as small as possible. Because of the triangulation equations, for a specific sensor type with common specifications of range, resolution and detector parameters, the sensor package size becomes larger as stand off increases. Therefore, it is usually desirable to select a sensor with enough standoff for clearance, without selecting excessive stand off. From an optical point of view, sensor resolution and accuracy are best when the surface is closest to the sensor. Sensor specifications for accuracy and resolution should be stated at the far end of the measuring range to represent the worst-case figures, and will improve when the surface is closer to the sensor.

Measurement Range, MR
The range over which the sensor gives a valid distance output signal. The range is given as an absolute value.

Spot size at SO
The value given relates to the diameter of the spot containing 90 % of the light energy.

Triangulation Angle at SO
The angle between the laser beam and the sensor viewing axis.

Courtesy: *LMI Technologies Inc. USA.*

A.3: Terminology related to the image sensor used in the thesis

Autosaturation time t_{auto}: Longest possible integration time, where the dark signal consumes the complete output voltage range. Units: s

Charge conversion factor (C_{eff}): The ratio between photo charge at the pixels and output voltage (Effective capacitance). units: fF.

Dark current (Idark): (apparent) photodiode current in the dark, per pixel or normalized per unit area. Units: A or A/cm^2

Dark signal (Vdark): (apparent) signal voltage [drop] in the dark, due to dark current due to dark current. Units: V or V/s

Fill factor (FF): Ratio between the light sensitive pixel area and the total pixel area (=100 % - obscuration factor)

Quantum efficiency (QE): Ratio between the number of generated electrons and the number of "impinging photons". = SR * hν/q. Units: %

Sensitivity: Output (V/s) versus input (W/m^2). Units: $V.m^2/W.s$

Spectral response (SR): Ratio of current and incoming light power for a given wavelength. Units: A/W

Source: B. Dierickx- Fillfactory : Photonics West 2000 short course: Gratefully acknowledged.

A.4: Glossary of Machine Vision terms related /used in the thesis
(Source: 'Datatranslation' is gratefully acknowledged)

http://www.datx.com/solution_center_mach_vision/Glossary-of-Machine-vision.pdf

Accuracy – The extent to which a machine vision system can correctly measure or obtain a true value of a feature. The closeness of the average value of the measurements to the actual dimension.
Ambient Light – Light which is present in the environment of the imaging front end of a vision system and generated from outside sources. This light, unless used for actual scene illumination, will be treated as background noise by the vision system.
Analog – A smooth, continuous voltage or current signal or function whose magnitude (value) is the information. From the word "analogous," meaning "similar to."
Analog-to-Digital Converter (A/D) – A device which converts an analog voltage or current signal to a discrete series of digitally encoded numbers (signal) for computer processing.
Binary image – A black and white image represented as a single bit containing either zeros or ones, in which objects appear as silhouettes. The result of backlighting or thresholding.
Bit – An acronym for a BInary digiT. It is the smallest unit of information which can be represented. A bit may be in one of two states, on or off, represented by a zero or a one.
Bit Map – A representation of graphics or characters by individual pixels arranged in rows and columns. Black and white require one bit, while fancy high definition colour up to 32.
CCD (Charge Coupled Device) – A photo-sensitive image sensor implemented with large scale integration technology.
Centroid – The centre of mass of an object having a constant density, or of an object having varying density, weighted by the gray scale value.
Collimate – To produce light with parallel rays.
Collimated Lighting – Radiation from a given point with every light ray considered parallel. In actuality, even light from a very distant point source (i.e. a star) diverges somewhat. Note that all collimators have some aberrations.
Depth-of-Field – The range of an imaging system in which objects are in focus.
Depth Perception (3D) – Measurement of the third dimension of an object or scene.
Digital Image – A video image converted into pixels. The numeric value of each pixel's value can be stored in a computer memory for subsequent processing and analysis.
Digitization – Sampling and conversion of an incoming video or other analog signal into a digital value for subsequent storage and processing.
Dynamic Range – The measure of the range light sensitivity a sensor is able to reproduce, from the darkest to the brightest portion of a scene. Usually expressed in decibels.
Fiducial – A line, mark or shape used as a standard of reference for measurement or location.
Field – The set of either the even or odd lines in a video image. The odd plus the even field comprise one video frame. A field is scanned every 1/60th of a second.
Field-of-View – The 2D area which can be seen through the optical imaging system.
Focal Length – The distance from a lens' principal point to the corresponding focal point on the object.
Focal Plane – Usually found at the image sensor, it is a plane perpendicular to the lens axis at the point of focus.
Focus – The point at which rays of light converge for any given point on the object in the image. Also called the focal point.
Height/Range – Object profile is usually measured by changes in range or distances from the sensor. 3D techniques are usually used.
High Speed Imaging – Image capture near, at or above 1800 parts per minute.
Holography – Optically recording of the interference pattern from two coherent waves which forms a 3 dimensional record or hologram.
Hybrid Electro-Optic Sensor – A silicon sensor fabricated in a configuration to match spatial information generated by the imaging system, such as a PSD (position sensitive detector), concentric rings, pie shapes and others.
Image – Projection of an object or scene onto a plane (i.e. screen or image sensor).
Image Analysis – Evaluation of an image based on its features for decision making.
Image Capture – The process of acquiring an image of a part or scene, from sensor irradiation to acquisition of a digital image.

Image Enhancement – Image processing operations which improve the visibility of image detail and features. Usually performed for humans.
Image Formation - Generation of an image of an object or scene on the imaging sensor. It includes effects from the optics, filters, illumination and sensor itself.
Image Plane – The plane surface of the imaging sensor, perpendicular to the viewing direction, at which the optics are focused.
Image Processing – Digital manipulation of an image to aid feature visibility, make measurements or alter image contents.
Incident Light – Light which falls directly onto an object.
Inspection – Non-destructive examination of a workpiece to verify conformance to some criteria.
I/O (Input/Output) – Data either entering or leaving a system.
Laplacian Operator – The sum of the second derivatives of the image intensity in both the x and y directions is called the Laplacian. The Laplacian operator is used to find edge elements by locating points where the Laplacian in zero.
Lens Types – The lenses most commonly used in machine vision are: 35mm, CCTV, Copying, Cylindrical, Enlarger, Micrographic, Video, and Wide Angle.
LIDAR (Light Detection And Ranging) – A system that uses light instead of microwaves for range and tracking measurements. LADAR uses a laser light source to measure velocity, altitude, height, range or profile.
Laser illumination – Lighting an object with a laser source for frequency selection, pulse width (strobe) control or for accurate positioning.
Line(s) of Light – One or more light stripes projected at a known angle onto the object.
Deformation of this type of structured light results in 3D information in a 2D image.
Line Scan Camera – A solid state video camera consisting of a single row of pixels. Also called a linear array camera.
Machine Vision – The use of devices for optical non-contact sensing to automatically receive and interpret an image of a real scene, in order to obtain information and/or control machines or processes.
Measurement – Verification that a workpiece conforms to specified tolerances, such as dimensions, colors or textures.
Moiré Interferometry – A method to determine 3D profile information of an object or scene, using interference of light stripes. Two identical gratings of known pitch are used. The first creates a shadow of parallel lines of light projected on the object. The second is placed in the imaging train, and superimposed on the shadow cast by the first grating, forming a moiré fringe pattern. Distance between the fringes or dark bands is directly related to range or profile. Varying the gap between the lines changes the sensitivity.
Moiré Pattern – A pattern resulting from the interference of light when gratings, screens or regularly spaced patterns are superimposed on one another. Two stacked window screens create this effect.
Moiré Topography – A contour mapping technique in which the object is both illuminated and viewed through the same grating. The resulting moiré fringes form contour lines of object elevation.
MOS Array – Metal Oxide Semiconductor camera array sensor with random addressing capability, rows and columns of photodiodes and charge sent directly from the photodiode to the camera output.
Object – The 3D item to be imaged, gauged or inspected.
Object Features – Any characteristic that is descriptive of an image or region, and useful for distinguishing one from another. A feature may be any measurable item such as length, size, number of holes, surface texture amount or center of mass.
Object Plane – An imaginary plane at the object, which is focused by the optical system at the image plane on the sensor
PAL (Phase Alternation Line) – A 50 Hz composite color video standard used in many parts of the world.
Photodiode – A single photoelectric sensor element, either used stand-alone or a pixel site, part of a larger sensor array.
Photometry – Measurement of light which is visible to the human eye (photopic response).
Pixel – An acronym for "picture element." The smallest distinguishable and resolvable area in an image. The discrete location of an individual photo-sensor in a solid state camera.
Pixel Counting – A simple technique for object identification representing the number of pixels contained within its boundaries.

Positioning Equipment – Used to bring the part into the field of view, or to translate when multiple images or views are required.
Precision – The degree of spread or deviation between each measurement of the same part or Feature.
Processing Speed – A measure of the time used by a vision system to receive, analyze and interpret image information. Often expressed in parts per minute.
Profile – The 3D contour of an object.
Range map rate -
Range Measurement – Determination of the distance from a sensor to the object.
Raster Scan – A scanning pattern, generally from left to right while progressing from top to bottom of the imaging sensor or the display monitor. Generally comprised of two fields composed of odd and even lines.
Real Time Processing – In machine vision, the ability of a system to perform a complete analysis and take action on one part before the next one arrives for inspection.
Reflection – The process by which incident light leaves the surface from the same side as it is illuminated.
Region – Area of an image focused on for image processing operations. See *Region of Interest, ROI.*
Region of Interest (ROI) – See *Region.*
Registration – The closeness of the part to the actual position expected for image acquisition.
Repeatability – The ability of a system to reproduce or duplicate the same measurement. The total range of variation of a dimension is called the 6-sigma repeatability. See *Precision*.
Resolution – A basic measurement of how much information is on the screen. Higher resolution means much more detail in the image.
Resolution, Pixel Grayscale – The number of resolvable shades of gray (i.e. 256).
Resolution, Image – The number of rows and columns of pixels in an image.
Resolution, Spatial – A direct function of pixel spacing. Pixel size relative to the image FOV (field-of-view) is key.
Resolution, Feature– The smallest object or feature in an image which may be sensed.
Resolution, Measurement – The smallest movement measurable by a vision system.
Rotation – Translation of a part about its center axis from the expected orientation in X and Y space. Expressed in degrees.
Scene – The object and a background in its simplest form. A portion of space imaged by a vision system for investigation or measurement.
Scene Analysis – Performing image processing and pattern recognition on an entire image.
Scheimpflug condition: When a lens is used to form an image of a sloping object, the object plane, the image plane and the median plane along the lens will all meet at a common point. This method of focus compensation is called schiempflug condition.(information belongs to a different source)
Segmentation – The process of dividing a scene into a number of individual objects or contiguous regions, differentiating them from each other and the image background.
Shading – The variation of the brightness or relative illumination over the surface of an object, often caused by color variations or surface curvature.
Shape – An object characteristic, often referring to its spatial contour.
Shape from Shading – A 3D technique that uses shadows from interaction of the object and the light source to determine shape.
Size – An object characteristic typically measured by x and y dimensions. Size may be expressed in pixels, the system calibrated units of measure or classes or size groups.
Smart Camera – A complete vision system contained in the camera body itself, including imaging, image processing and decision making functions.
Solid-State Camera – A camera which uses a solid state integrated circuit chip to convert incident light or other radiation into an analog electrical signal.
Span – The allowance of gray level acceptance for thresholding, adjustable from black to white from 0 to 100%.
Spatial Light Modulator – A transparent screen used in optical computer systems to introduce an image into the optical processing path. Similar to liquid crystal computer display screens, their resolution approaches 512x512 and grayscale imaging 8 bits. Also SLM.
Spectral Analysis – Evaluation of the wavelength composition of object irradiance.

Spectral Characteristics – The unique combination of wavelengths of light radiated from a source or transmitter or reflected from an object.
Speckle: result of the interference of waves originating from scatter centre centres illuminated by a coherent laser source. (This information is not related to this source.)
Spectral Response – The characteristic of a sensor to respond to a distribution of light by wavelength in the electromagnetic spectrum.
Specular Reflection – Light rays that are highly redirected at or near the same angle of incidence to a surface. Observation at this angle allows the viewer to "see" the light source.
Stereo (Passive) – For imaging, the use of two cameras, offset by a known distance and angle, to image the same object and provide range, depth or 3D information. Active stereo uses a controlled or structured light source to provide 3D data.
Stereo Photogrammetry – See *Shape from Shading*.
Stereoscopic Approach – The use of triangulation between two or more image views from differing positions. Used to determine range or depth.
Structured Light – Points, lines, circles, sheets and other projected configurations used to directly determine shape and/or range information by observing their deformation as it intersects the object in a known geometric configuration.
Subpixel Resolution – Mathematical techniques used on gray scale images to resolve an edge location to less than one pixel. A one tenth pixel resolution is reasonable in the factory.
System Performance Measures – Accuracy, precision or repeatability, and alpha and beta risk for a given throughput rate specify the performance of a vision system.
Sync – The portion of a video signal indicating either the end of a field or end of a line of video information.
Thresholding – The process of converting gray scale image into a binary image. If the pixel's value is above the threshold, it is converted to white. If below the threshold, the pixel value is converted to black.
Triangulation – A method of determining distance by forming a right triangle consisting of a light source, camera and the object. The distance or range can be calculated if the camera-to-light source distance and the incident to reflected beam angle are both known. Based on the Pythagorean relation.
Visible Light – The region of the electromagnetic spectrum in which the human retina is sensitive, ranging from about 400 to 750 nm in wavelength.
Vision Engine – Analyzes the image and makes decisions, using a very fast processor inside a computer. It performs dedicated evaluation of the pre-processed image data to find features and make measurements. Unlike a personal computer, the vision engine is built for speed, not flexibility
Wavelength – The distance covered by one cycle of a sinusoidally varying wave as it travels at or near the speed of light. It is inversely proportional to frequency.
Window – A selected portion of an image or a narrow range of gray scale values.
Windowing – Performing image processing operations only within a predefined window or area in the image.
X-ray – A portion of the electromagnetic spectrum beyond the ultraviolet with higher frequency and shorter wavelengths. Able to penetrate solid objects for internal, non-destructive evaluation.

Appendix B

Table B.1: *Description of the imager signals (Please refer to Chapter 5)*

Signal	Description
(i) *Input pins*	
RESN	*When L,* resets the Linear sensor
PHRES	Controls the input phase of the photodiode, image is acquired when this signal is high
LASR	Pulse to laser source
CIN	Input to 'START' the process
DIR	Dir: Direction, *L*=forward(up), *H*=reverse(down)
CLK	Signal to U/D counter, depending on the status (MUX) either this signal is fed to the counter or the tstclk input
TSTCLK	Test clock input to the counter for testing the counter independently
TSTCOUNTER	When *H*, enables the counter test independently
RESNCNTR	When *L,* resets the counter
RESNSR	When *L,* resets the shift register
SEL	Mode selection input: when *L*, load data mode: loads data into the shift register, in conjunction with the CKBIN signal. When H, shift register mode
CKBIN	Shift register clock
V_{th}	Threshold voltage input
V_{res}	Photodiode reset voltage
Q<0:11>	Device internal : 12 data bits for connecting to the shift register
Qin	Input to the shift register used in isolated testing
(ii)Output pins	
CO	Output of the up/down counter
COUT	*Carryout* of the linear sensor generated in each direction, when no pixel crosses the threshold
Qserial	Serial output of the shift register/ linear sensor

Table B2: *Pixel table in binary used in up/ down counting (Please refer to Chapter 6)*

Pixel No.	UP binary value	Down binary value
1	0000 0000 0001	1111 1111 1111
2	0000 0000 0010	1111 1111 1110
3	0000 0000 0011	1111 1111 1101
4	0000 0000 0100	1111 1111 1100
5	0000 0000 0101	1111 1111 1011
6	0000 0000 0110	1111 1111 1010
7	0000 0000 0111	1111 1111 1001
8	0000 0000 1000	1111 1111 1000
9	0000 0000 1001	1111 1111 0111
10	0000 0000 1010	1111 1111 0110
11	0000 0000 1011	1111 1111 0101
12	0000 0000 1100	1111 1111 0100
13	0000 0000 1101	1111 1111 0011
14	0000 0000 1110	1111 1111 0010
15	0000 0000 1111	1111 1111 0001
16	0000 0001 0000	1111 1111 0000
17	0000 0001 0001	1111 1110 1111
18	0000 0001 0010	1111 1110 1110
19	0000 0001 0011	1111 1110 1101
20	0000 0001 0100	1111 1110 1100
21	0000 0001 0101	1111 1110 1011
22	0000 0001 0110	1111 1110 1010
23	0000 0001 0111	1111 1110 1001
24	0000 0001 1000	1111 1110 1000
25	0000 0001 1001	1111 1110 0111
26	0000 0001 1010	1111 1110 0110
27	0000 0001 1011	1111 1110 0101
28	0000 0001 1100	1111 1110 0100
29	0000 0001 1101	1111 1110 0011
30	0000 0001 1110	1111 1110 0010
31	0000 0001 1111	1111 1110 0001

Table B.3: *Pixel position measurement and 'difference' readings (Please refer to the Chapter 6)*

pixel	binary	bin2dec	div/256 for loop =128	difference
pixel				
1	000100000111	263	1.027343750	
	100010001	273	1.066406250	0.039062500
	100001100	268	1.046875000	-0.019531250
	100000110	262	1.023437500	-0.023437500
	100000010	258	1.007812500	-0.015625000
	100001000	264	1.031250000	0.023437500
	100000011	259	1.011718750	-0.019531250
	100001001	265	1.035156250	0.023437500
	100011100	284	1.109375000	0.074218750
	100100010	290	1.132812500	0.023437500
	100100011	291	1.136718750	0.003906250
	100100101	293	1.144531250	0.007812500
	100100110	294	1.148437500	0.003906250
	100100101	293	1.144531250	-0.003906250
	100100010	290	1.132812500	-0.011718750
	100100111	295	1.152343750	0.019531250
	100100110	294	1.148437500	-0.003906250
	100100111	295	1.152343750	0.003906250
	100101100	300	1.171875000	0.019531250
	100100110	294	1.148437500	-0.023437500
	100011011	283	1.105468750	-0.042968750
	100010011	275	1.074218750	-0.031250000
	100010000	272	1.062500000	-0.011718750
	100010001	273	1.066406250	0.003906250
	100011010	282	1.101562500	0.035156250
	100100001	289	1.128906250	0.027343750
	100101010	298	1.164062500	0.035156250
	100110111	311	1.214843750	0.050781250
	101000001	321	1.253906250	0.039062500
	101000111	327	1.277343750	0.023437500
	101001001	329	1.285156250	0.007812500
	101000110	326	1.273437500	-0.011718750
	101000100	324	1.265625000	-0.007812500
	101001111	335	1.308593750	0.042968750
	101010100	340	1.328125000	0.019531250
	101010111	343	1.339843750	0.011718750
	101011111	351	1.371093750	0.031250000
	101100111	359	1.402343750	0.031250000
	101110100	372	1.453125000	0.050781250
	101111100	380	1.484375000	0.031250000
	110000111	391	1.527343750	0.042968750
	110011001	409	1.597656250	0.070312500
	110010001	401	1.566406250	-0.031250000
	110010011	403	1.574218750	0.007812500
	110010010	402	1.570312500	-0.003906250
	110001111	399	1.558593750	-0.011718750
	110001000	392	1.531250000	-0.027343750
	110010100	404	1.578125000	0.046875000
	110100001	417	1.628906250	0.050781250
	110011111	415	1.621093750	-0.007812500

110101000	424	1.656250000	0.035156250
110101110	430	1.679687500	0.023437500
110111011	443	1.730468750	0.050781250
110111101	445	1.738281250	0.007812500
111000010	450	1.757812500	0.019531250
111000100	452	1.765625000	0.007812500
111001010	458	1.789062500	0.023437500
110111101	445	1.738281250	-0.050781250
110110111	439	1.714843750	-0.023437500
110111101	445	1.738281250	0.023437500
111000010	450	1.757812500	0.019531250
111000111	455	1.777343750	0.019531250
111010010	466	1.820312500	0.042968750
111010111	471	1.839843750	0.019531250
111011100	476	1.859375000	0.019531250
111010100	468	1.828125000	-0.031250000
111010111	471	1.839843750	0.011718750
111010100	468	1.828125000	-0.011718750
111010011	467	1.824218750	-0.003906250
111010110	470	1.835937500	0.011718750
111010111	471	1.839843750	0.003906250
111010011	467	1.824218750	-0.015625000
111011010	474	1.851562500	0.027343750
111011000	472	1.843750000	-0.007812500
111001101	461	1.800781250	-0.042968750
111001100	460	1.796875000	-0.003906250
111001011	459	1.792968750	-0.003906250
111001110	462	1.804687500	0.011718750
111010010	466	1.820312500	0.015625000
111001011	459	1.792968750	-0.027343750
111001110	462	1.804687500	0.011718750
111001101	461	1.800781250	-0.003906250
111010100	468	1.828125000	0.027343750
111010011	467	1.824218750	-0.003906250
111010001	465	1.816406250	-0.007812500
111001011	459	1.792968750	-0.023437500
111001101	461	1.800781250	0.007812500
111010010	466	1.820312500	0.019531250
111010010	466	1.820312500	0.000000000
111011000	472	1.843750000	0.023437500
111001011	459	1.792968750	-0.050781250
111001001	457	1.785156250	-0.007812500
111001100	460	1.796875000	0.011718750
111001110	462	1.804687500	0.007812500
111011000	472	1.843750000	0.039062500
111100000	480	1.875000000	0.031250000
111100010	482	1.882812500	0.007812500
111101101	493	1.925781250	0.042968750
111101011	491	1.917968750	-0.007812500
111100010	482	1.882812500	-0.035156250
111101000	488	1.906250000	0.023437500
111100100	484	1.890625000	-0.015625000
111100110	486	1.898437500	0.007812500
111100111	487	1.902343750	0.003906250
111101111	495	1.933593750	0.031250000
111100110	486	1.898437500	-0.035156250

	111110001	497	1.941406250	0.042968750
	111110111	503	1.964843750	0.023437500
pixel 2	001000000101	517	2.019531250	0.054687500
	1000001010	522	2.039062500	0.019531250
	1000001001	521	2.035156250	-0.003906250
	1000001001	521	2.035156250	0.000000000
	1000001000	520	2.031250000	-0.003906250
	1000000101	517	2.019531250	-0.011718750
	1000010011	531	2.074218750	0.054687500
	1000010011	531	2.074218750	0.000000000
	1000011101	541	2.113281250	0.039062500
	1000011111	543	2.121093750	0.007812500
	1000100000	544	2.125000000	0.003906250
	1000011001	537	2.097656250	-0.027343750
	1000011110	542	2.117187500	0.019531250
	1000100001	545	2.128906250	0.011718750
	1000101100	556	2.171875000	0.042968750
	1001100111	613	2.394531250	0.222656250
	1001100100	612	2.390625000	-0.003906250
	1001011101	605	2.363281250	-0.027343750
	1001101101	621	2.425781250	0.062500000
	1010010010	658	2.570312500	0.144531250
	1010010110	662	2.585937500	0.015625000
	1010000100	644	2.515625000	-0.070312500
	1001111011	635	2.480468750	-0.035156250
	1010011000	664	2.593750000	0.113281250
	1010011100	668	2.609375000	0.015625000
	1010100111	679	2.652343750	0.042968750
	1010110010	690	2.695312500	0.042968750
	1010110111	695	2.714843750	0.019531250
	1010110110	694	2.710937500	-0.003906250
	1010111000	696	2.718750000	0.007812500
	1010111011	699	2.730468750	0.011718750
	1010111100	700	2.734375000	0.003906250
	1011000000	704	2.750000000	0.015625000
	1011000010	706	2.757812500	0.007812500
	1011001100	716	2.796875000	0.039062500
	1011010010	722	2.820312500	0.023437500
	1011011000	728	2.843750000	0.023437500
	1011011001	729	2.847656250	0.003906250
	1011010111	727	2.839843750	-0.007812500
	1011011100	732	2.859375000	0.019531250
	1011011010	730	2.851562500	-0.007812500
	1011010101	725	2.832031250	-0.019531250
	1011011000	728	2.843750000	0.011718750
	1011011110	734	2.867187500	0.023437500
	1011100011	739	2.886718750	0.019531250
	1011101011	747	2.917968750	0.031250000
	1011110000	752	2.937500000	0.019531250
	1011110101	757	2.957031250	0.019531250
	1011110111	759	2.964843750	0.007812500
	1011110101	757	2.957031250	-0.007812500
	1011111001	761	2.972656250	0.015625000
	1011111011	763	2.980468750	0.007812500
	1011111011	763	2.980468750	0.000000000

	1100000001	769	3.003906250	0.023437500
	1100001001	777	3.035156250	0.031250000
pixel 3	001100000101	773	3.019531250	-0.015625000
	1100011001	793	3.097656250	0.078125000
	1100101000	808	3.156250000	0.058593750
	1100100101	805	3.144531250	-0.011718750
	1100101010	810	3.164062500	0.019531250
	1100100101	805	3.144531250	-0.019531250

Table B.4: *Specifications of the device*

Parameter	**Specification**
process	AMS .35 µm CMOS 3-metal 2-poly-Si
Linear sensor size	1.3mm
Array size	31 pixels
Pixel size	45 µm x 40 µm
Number of transistors per pixel	40
Fill factor	~27%
Photodiode area	486 μm^2
capacitance	55.15 fF @ 2V
responsivity	0.15 A/W
reset voltage	2.0 V
Threshold Voltage	1.5 V
Background current	0.06 fA/μ^2
Conversion factor	3.4 $\mu V/e^-$
Measured frequency of pulses on bit-line	8 MHz (125 ns pulse width)
Single processing cycle	7.8 µs/cycle
Complete processing cycle (for N thresholds)	N x (11 µs/cycle) = 1.408 ms (for 128 thresholds)
Standard deviation (for N=128)	0.0329 pixels (1.48 µm)
Sensor Accuracy (N=128) ±1σ	6.6% (2.96 µm)
Sensor resolution	~ 9 bits (5 + 4)
Spot size	~ 250 µm
Max. Light power density on the linear sensor	1.8 $\mu W/cm^2$