

# DEPARTMENT OF INFORMATION AND COMMUNICATION TECHNOLOGY

38050 Povo – Trento (Italy), Via Sommarive 14 http://www.dit.unitn.it

## FAST ESTIMATION OF A/D CONVERTER NONLINEARITIES

Fabrizio Stefani, Antonio Moschitta, David Macii, Paolo Carbone, Dario Petri

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## **Fast Estimation of A/D Converter Nonlinearities**

F. Stefani<sup>1</sup>, A. Moschitta<sup>1</sup>, D. Macii<sup>2</sup>, P. Carbone<sup>1</sup>, D. Petri<sup>2</sup>

<sup>1</sup>DIEI, University of Perugia – Via G. Duranti, 93 – 06125 Perugia (PG), Italy Phone: +39 075 5853933; Fax: +39 075 5853654; e-mail: {stefani, moschitta, carbone}@diei.unipg.it <sup>2</sup>DIT, University of Trento – Via Sommarive, 14 – 38050 Trento (TN), Italy Phone: +39 0461 883902; Fax: +39 0461 882093; e-mail: {macii, petri}@dit.unitn.it

**Abstract** – This paper deals with an innovative strategy to shorten the record size required to estimate the Integral Non-Linearity (INL) of Analog-to-Digital Converters (ADC's) through the so-called Sinewave Histogram Test (SHT). Such a size reduction is achieved by low-pass filtering the collected sequences of test samples using a simple moving average filter. After some preliminary simulations, the validity of the proposed approach have been confirmed by some experimental results.

#### I. Introduction

Nowadays, characterization and testing activities are a major factor of cost in integrated circuit (IC) manufacturing. In fact, testing mixed-signal circuits may cover nearly 50% of the whole production budget [1]. Among all the possible testing procedures, Histogram Tests are probably the best-known strategies to characterize the linearity features of an ADC. These techniques estimate the converter transition levels by analyzing the ADC output codes when the stimulus has a known probability density function [2]. The main advantage of Histogram based Tests, such as the Sinewave Histogram Test (SHT), is that the estimator variance can be made arbitrarily close to the Cramer-Rao lower bound, while the theoretical and computational complexity of the algorithm is very low [3][[5]. Unfortunately, for ADC with more than 12 bits of nominal resolution, achieving an estimator accuracy lower than a Least Significant Bit (LSB) may require data records consisting of millions of test samples [6]. Therefore, an accurate INL estimation can be very expensive and time-consuming, because of the large data acquisition and transfer times.

Several techniques have been proposed to decrease the total number of samples required by the SHT. Some of them are based on a frequency domain analysis of the estimated INL [6][7]. Others rely on proper analytical models describing the dependence of the INL patterns on the code bins [8][9]. In this paper, it is shown that the constraint on the record size can be relaxed by applying moving average (MA) filtering upon the SHT results obtained with a small size data set. In particular, the proposed technique allows a fast and very accurate estimation of the low frequency code component (LCF) of the INL sequence, which often represents a major information about converter nonlinearity [8]. Nevertheless, the high frequency code (HFC) component of the INL can still be estimated with a given accuracy, if a suitable tradeoff is found between the length of the MA filter and the size of the data record employed in the test.

The paper is organized as follows. At first, the general SHT design criteria are shortly recalled. Then, the theoretical effect of MA filtering on SHT outcomes is described and compared with meaningful simulation results. Finally, the results of an experimental validation of the proposed testing procedure are reported and commented.

#### II. Theoretical Analysis

#### A. The design of the Sinewave Histogram Test

The SHT is based on the acquisition of a large number of data obtained by sampling a high-accuracy sinewave affected by a known amount of Additive White Gaussian Noise (AWGN). In fact, not only can sinusoidal stimuli be generated easily, but also they allow the frequency characterization of the ADC under test. In SHT, the converter transition voltages  $T_k$ , k=1,...,N-1, are estimated by means of a two-step procedure. At first, collected data are used to build a cumulative histogram in which the value  $c_k$  associated with the k-th column of the histogram represents the total number of acquired samples exhibiting an output code equal to or lower than k. Then, the corresponding transition level  $T_k$  is estimated by inverting the known probability distribution function of the input test stimulus. In fact, it has been proved that the estimate of the k-th ADC transition level  $\hat{T}_k$  is given by [2]:

$$\hat{T}_k = d - A\cos\left(\pi \frac{c_k}{M}\right) \qquad k = 1, \dots, N - 1,$$
(1)

where A and d are the amplitude and the offset of the sinewave, respectively, M is the length of the collected record, and N is the number of ADC output codes. The SHT accuracy when a sinusoidal stimulus is affected by an AWGN has been already analyzed in previous research works, showing that the AWGN introduces both a random contribution and a bias into the estimator uncertainty [10],[11]. The estimator bias can be made negligible by overdriving the ADC, i.e. by applying a sinewave amplitude suitably higher than the ADC Full Scale (FS) [10]. Conversely, for large values of M, the variance of (1) is given by [4]:

$$\sigma_{T_k}^2 \cong \frac{1.78\sigma}{M} \sqrt{A^2 - T_k^2} \le 1.78 \frac{A\sigma}{M}, \quad A \ge |T_k|, \quad k = 1,..., N-1,$$
 (2)

 $\sigma$  being the standard deviation of the AWGN. Observe that the estimator variance tends to zero as M increases. Moreover, if the AWGN estimator bias is made negligible, (2) can be inverted to obtain the data record size M as a function of the target SHT accuracy [10], thus obtaining:

$$M \ge \frac{1.78A\sigma K_{\nu}^{2}}{U_{INL}^{2}},\tag{3}$$

where  $U_{INL}$  is the target expanded INL uncertainty and  $K_{\nu}$  is the coverage factor corresponding to a degree of confidence  $\nu$  [11].

#### B. Effect of Moving-Average Filtering on SHT results

The traditional SHT procedure does not take advantage of the characteristics of the INL pattern, which may be decomposed in two components, a LCF and a HCF ones [5]. The idea behind this work is that the LCF component can be estimated by observing that the estimated *INL* sequence can be written as:

$$I\hat{N}L[k] = INL[k] + e[k], \qquad k=1,...N-1, \tag{4}$$

where it has been shown that the estimation error  $e[\cdot]$  can be assumed to be a white sequence of random variables as long as the input noise level is lower than the code bin width  $\Delta$  [6]. Thus, an appropriate low-pass filtering of the INL sequence provided by the SHT may remove high-frequency random contributions affecting the estimator, leading to a significant accuracy improvement in the estimation of the LCF-INL pattern.

Consider, for instance, the sequence  $INL[\cdot]$  obtained by applying a low-pass moving-average (MA) filter over P estimated INL values related to adjacent code bins:

$$\overline{INL}[k] = \frac{1}{P} \sum_{i=-(P-1)/2}^{(P-1)/2} INL[k+i], \qquad k = (P-1)/2, \dots, N-1-(P-1)/2, P \text{ odd}$$
 (5)

It can easily be shown that the variance  $\sigma_{\overline{\mathit{INL}}}^2$  at the output of the MA filter is

$$\sigma_{\overline{INL}}^2 \cong \sigma_e^2 / P, \quad \sigma < \Delta.$$
 (6)

where  $\sigma_e^2$  represents the variance of the estimation error. Thus, if the code bin width is smaller than the input noise level [9], the MA filtering leads to an LCF-INL estimator variance that is proportional to 1/MP. Consequently, as long as the estimator bias is negligible, the same estimator uncertainty of an SHT performed on M'=MP samples may be achieved by averaging over P values the SHT results obtained using a record of M samples.

Notice that, if the input noise level exceeds the code bin width, the estimation errors in adjacent transition levels are correlated. Hence, the resulting  $\sigma_{INL}^2$  could be quite greater than (6). Nevertheless, the record size M may be noticeably lower than that usually required by conventional SHT.

One limitation of the proposed approach is that while the filtering process does not affect the LCF component of the INL pattern, the HCF content could be considerably smoothed if large values of P are used. Thus, a suitable tradeoff between the data record size M and the filter length P must be find . As a rule of thumb, in order to minimize the distortion introduced by filtering, 1/P should be at least

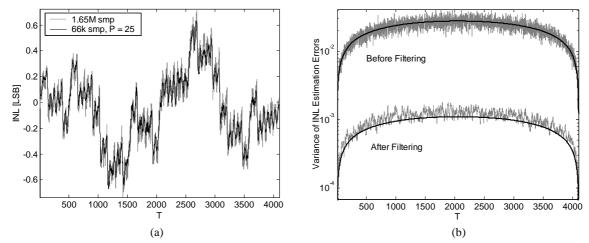


Fig. 1: (a) Estimated INL patterns of a simulated 12-bit ADC, obtained with a conventional SHT for M' = 1.650.000 (grey curve) and a MA filtered SHT for M=66.000, P=25 (black curve). (b) INL estimator error variances for the MA filtered SHT, both before and after averaging; the black curves correspond to the theoretical expressions (2) and (5), while the grey curves are simulation results.

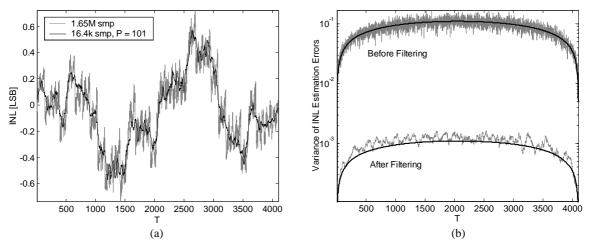


Fig. 2: (a) Estimated INL patterns of a simulated 12-bit ADC, obtained with a conventional SHT for M' = 1.650.000 (grey curve) and a MA filtered SHT for M=16.400 and P=101 (black curve). (b) INL estimator error variances for the MA filtered SHT, both before and after averaging; the black curves correspond to the theoretical expressions (2) and (5), while the grey curves are simulation results.

one order of magnitude larger than the bandwidth of the INL sequence.

#### **III. Simulation Results**

The proposed test strategy has been applied to a simulated 12-bit ADC converter with a Full Scale FS=10 V. The maximum INL error has been set equal to 0.7 Least Significant Bits (LSB). In order to minimize the estimator bias, a 25 kHz sinewave with a small overdrive of 0.04 V and no offset (A=10.04 V, d=0.0 V) has been chosen for the test [10]. The AWGN superimposed to the sinewave has been assumed to have a standard deviation  $\sigma$ =0.5 LSB. The SHT has been initially designed to achieve a target expanded uncertainty  $U_{INL}$ =0.1LSB. Consequently, by assuming a coverage factor  $K_V$ =3, according to (3) the SHT requires a data record consisting of M'=1.650.000 samples. Alternatively, a faster test can be performed using only M=66.000 samples and a MA filter with length P=25. Fig. 1(a) shows the INL patterns estimated using both the conventional SHT and the MA filtered SHT as a function of the transition levels. Observe that the filtered results still provide a good estimate of the INL pattern, but using a data record size 25 times smaller. The estimator error variances for the SHT performed with M=66.000, before and after applying the MA filtering are plotted in Fig. 1(b). In

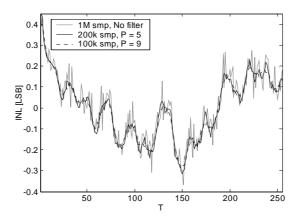
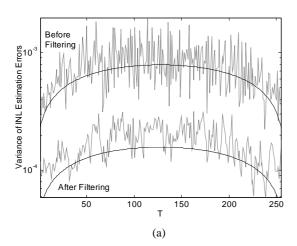


Fig. 3: INL patterns of the 8 bit ADC employed in an NI5911 digitizer, obtained with a conventional SHT and two fast MA-based SHT. The INL values are estimated using  $10^6$ ,  $2 \cdot 10^5$ , and  $10^5$  test data samples and with an appropriate MA filtering. In order to preserve the expected accuracy in the estimation process, the INL values obtained from the record consisting of  $2 \cdot 10^5$  data are averaged over P=5, whereas the results derived using  $10^5$  samples are averaged over P=9.

particular, both the theoretical variance values obtained from (2) and (5), and the simulation results are reported as a function of the transition levels. Notice that the SHT accuracy is actually improved by the low-pass filtering, and that the simulation-based results show a good agreement with the theoretical model. The analysis has been repeated for different values of M and P. In particular, Fig. 2(a) and 2(b) are obtained considering a SHT on M=16.400 samples, followed by a MA filtering with P=101. Again, Fig. 2(b) shows that the record size can be considerably reduced without affecting the estimator variance. However, in this case the estimated INL looks slightly distorted with respect to the pattern resulting from the conventional SHT (see Fig. 2(a)). This is due to the narrow bandwidth of the adopted MA filter (i.e. to the large value of P), which reduces the sensitivity of the test procedure to fast INL variations.

## **IV. Experimental Results**

In order to validate the results described in section II, several experiments have been performed to estimate the INL of an 8-bit ADC embedded in a NI 5911 high-speed digitizer. The device under test can be fully characterized using the default setting of the digitizer, i.e. a sampling rate equal to 100 Msamples/s and a Full Scale (FS) range equal to ±10 V. A 25 kHz low-distortion sinewave produced by a Stanford Research DS360 function generator has been used as input stimulus for the test. The number of samples and the amount of overdrive required by the procedure depend on the desired expanded uncertainty levels, and can be established after estimating the noise standard deviation  $\sigma$ . In the considered case,  $U_{\rm INL}$ =2.5% LSB and  $\sigma$ =0.052 V, so that the overdrive voltage is  $V_{od} \cong 0.45$  V, while the offset d of the waveform is assumed to be 0 V [2]. In order for the SHT random uncertainty to be lower than 4% LSB, according to (3) about 10<sup>6</sup> test samples should be collected. On the other hand, only 10<sup>6</sup>/P samples are required to estimate the same INL pattern with the same accuracy when the fast SHT procedure is applied. In Fig. 3 the estimated INL patterns using 10<sup>6</sup>, 2·10<sup>5</sup>, and 10<sup>5</sup> test samples are shown before and after the appropriate MA filtering operations. In order to achieve the same target estimation accuracy, the SHT results obtained from 10<sup>6</sup> samples are not filtered, whereas the INL values calculated using  $2.10^5$  and  $1.10^5$  test data, are averaged over P=5 and P=9 values, respectively. Observe that the low-frequency content of the INL pattern is estimated with good accuracy in all cases, whereas the high-frequency components are increasingly smoothed as the cut-off frequency of the MA filter decreases. The estimated and theoretical variances of the INL estimation errors before and after the averaging operations for P=5 and P=9 are shown in Fig. 4(a) and 4(b), respectively. Notice that while in the previously discussed simulation data sets case there is a very good accordance between theoretical and experimental variances, in present analysis, involving experimental data sets, the actual variance seems to be slightly larger than expected. Most probably, this is due to a certain amount of residual cross-correlation between subsequent INL estimators, which decreases the effectiveness of the averaging operation.



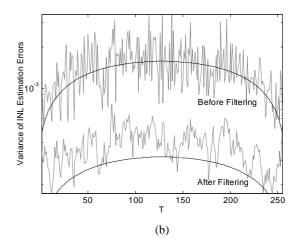


Fig. 4: INL estimator error variances for the MA filtered SHT performed on the ADC employed in an NI 5911 digitizer. In (a) the estimation variance is reported both before and after moving averaging over P=5 values, for a SHT run using  $2 \cdot 10^5$  samples and the corresponding error variances are reported. In (b), similar results are shown using only  $10^5$  samples and P=9. Like in Fig. 2, the black curves correspond to the theoretical variances resulting from (2) and (5), while the grey curves are based on experimental results.

#### V. Conclusions

In this paper a very simple strategy to speed up the INL estimation of high-resolution ADCs is presented. According to the proposed approach, by low-pass filtering the INL sequence estimated through the Sinewave Histogram Test, a remarkable accuracy improvement can be achieved, thus relaxing the usual record size requirements. In fact, since the INL estimation errors can be usually modeled as an almost white broadband process, a simple low-pass filter such as a moving average over an adequate number of adjacent INL values can greatly attenuate the high-frequency random contributions without affecting significantly the INL pattern. Simulations and experimental results in two different cases of study confirm that MA filtering can provide a considerable improvement in estimation accuracy, although such an improvement can be lower than expected when the input noise level is greater than the code bin width.

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